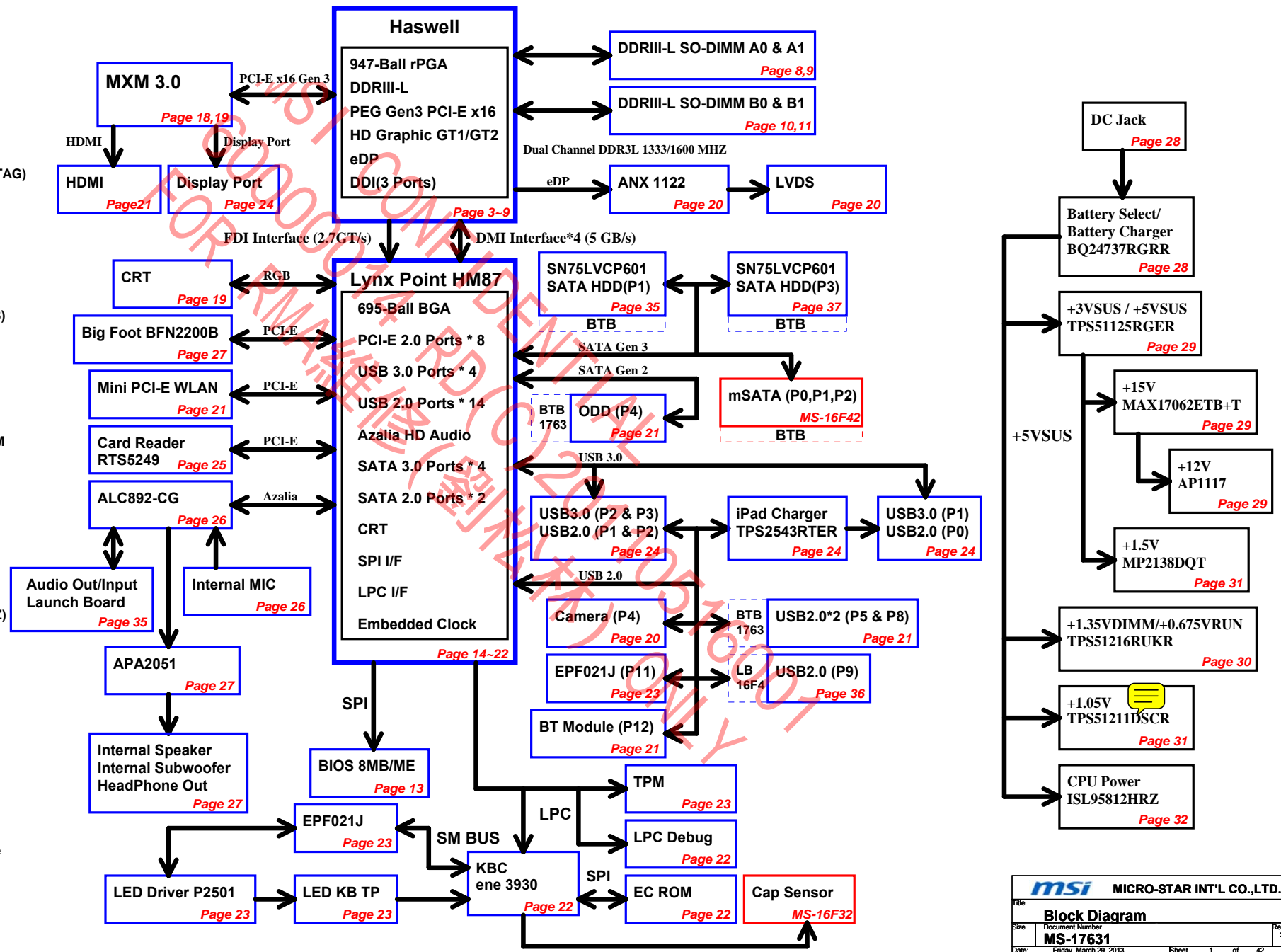


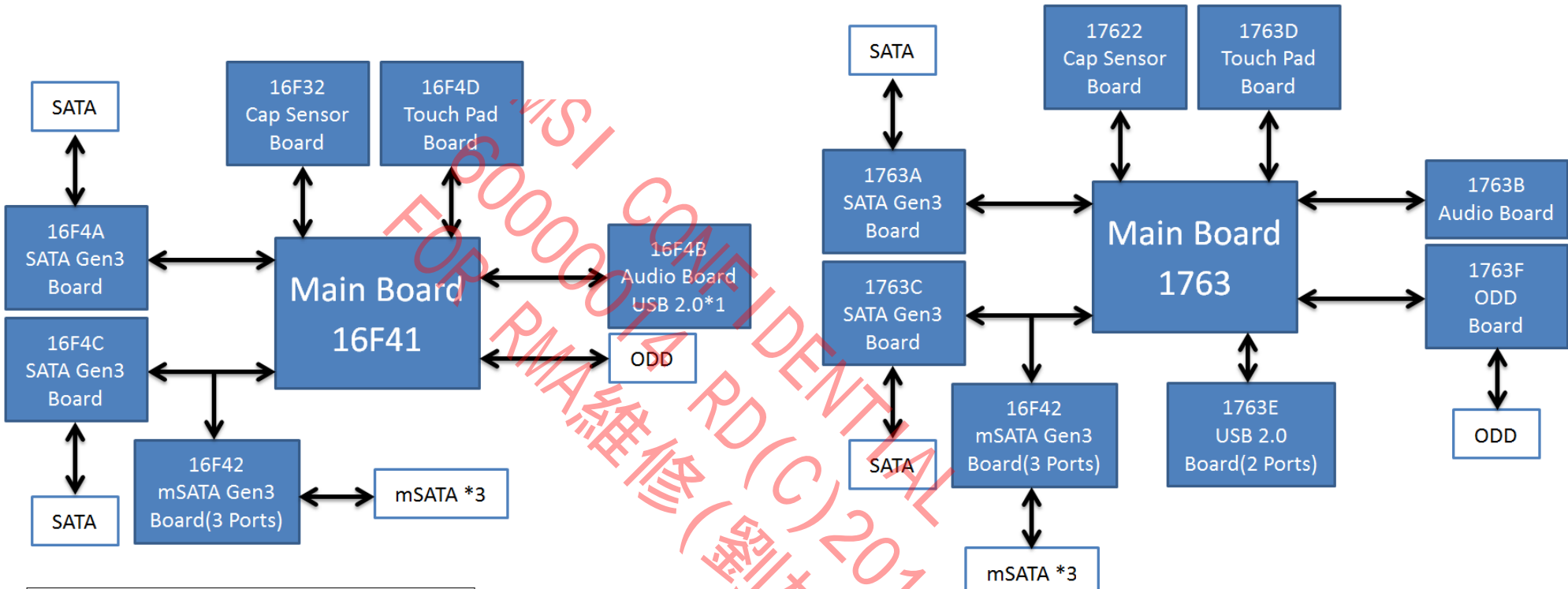
Shark Bay Platform

MS-1763M1 Ver 2.0 2013/03/19

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 Page 28:Battery Select/Charger
 Page 29:System Power
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 Page 31:+1.05VRUN/+1.5VRUN
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 Page 35:1763B_IO/Audio Board
 Page 36:1763C_HDD2
 Page 37:1763D_Touch Pad L/R Key
 Page 38:1763E_USB Connector
 Page 39:1763F_ODD Board
 Page 40:1763G_SPK_L_LED
 Page 41:1763H_SPK_R_LED
 Page 42:1763I_CDLED_LF
 Page 43:1763J_CDLED_RF
 Page 44:1763L_Power_Bottom
 Page 45:Impedance/Clock Distribution
 Page 46:Power on Sequency
 Page 47:Power Down & MXM Sequence
 Page 48:Power Diagram
 Page 49:Power Delivery Chart



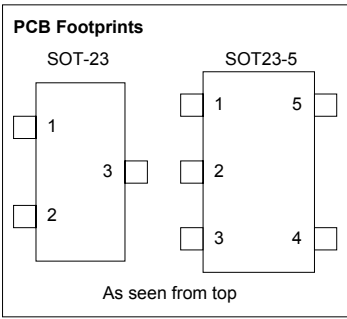
Board Diagram



Voltage Rails			
Power Plane	Voltage	Active In	Description
PWR_SRC	19V or 12 V	S0, S3-S5	Power Source
+5VALW	5V	S0, S3-S5	
+3VALW	3.3V	S0, S3-S5	
+5VSUS	5V	S0, S3	
+3VSUS	3.3V	S0, S3	
+1_35VDIMM	1.35V	S0, S3	DDR3L Power
+5VRUN	5V	S0	
+3VRUN	3.3V	S0	
+1_5VRUN	1.5V	S0	PCH Power for I/O
+12V_FAN	12V	S0	Fan Power
+15V	15V	S0	LED Keyboard Power
+0_675VRUN	0.675V	S0	
+1_05VRUN	1.05V	S0	
+VCC_CORE	1.2V	S0	Processor Core Power Rail

Net Naming Conventions
Suffix
= Active Low Signal
Prefix
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

Power States						
	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+V*SUS	+V*RUN
S0 (Full on)	High	High	High	On	On	On
S3 (Suspend to RAM)	Low	High	High	On	On	Off
S4 (Suspend to Disk)	Low	Low	High	On	Off	Off
S5 (Soft off)	Low	Low	Low	On	Off	Off

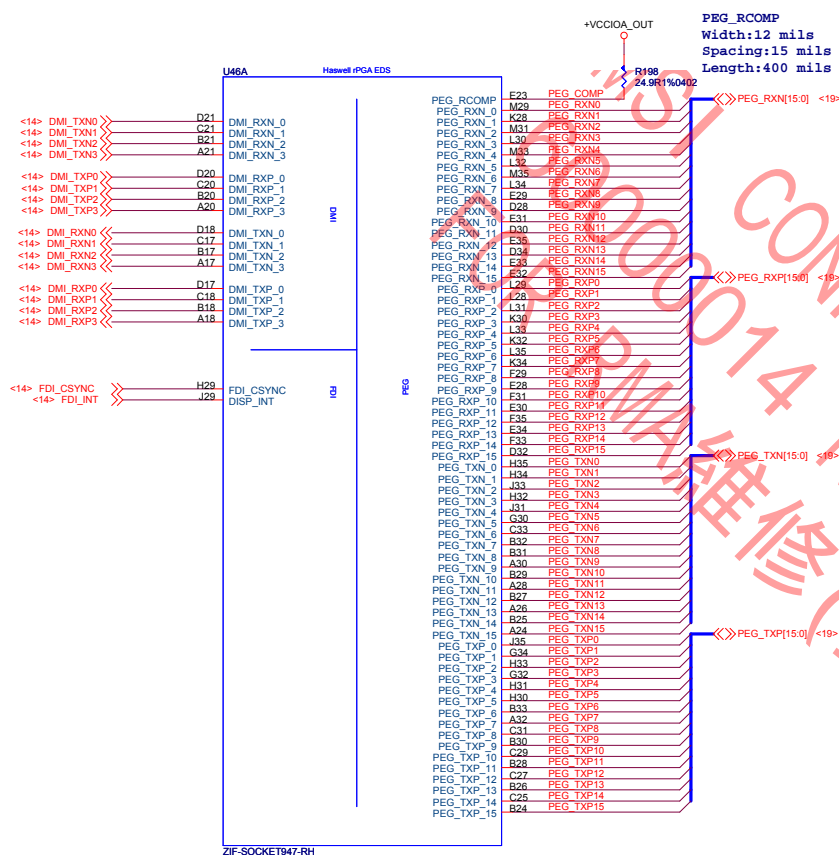
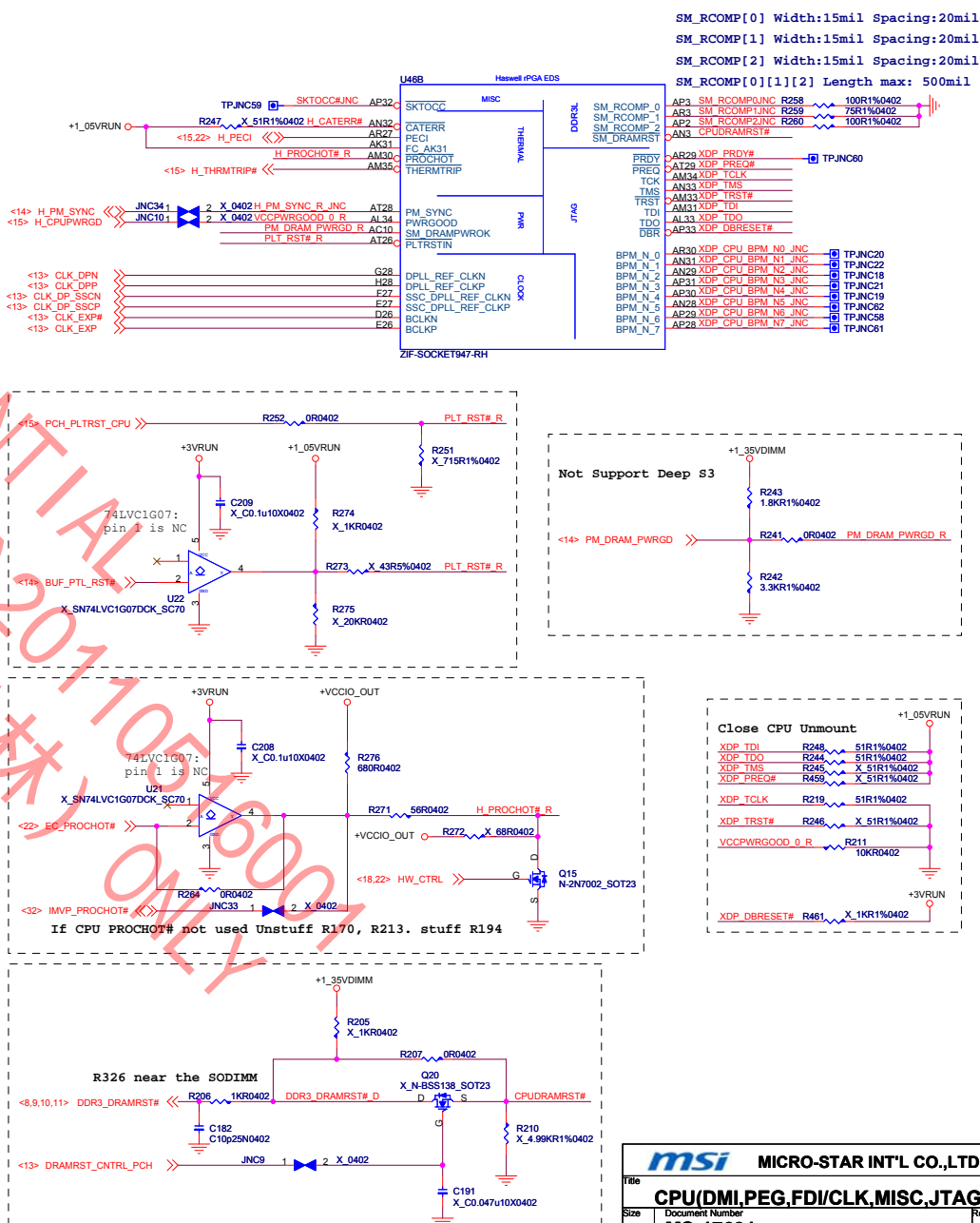


MS-17631 Change List

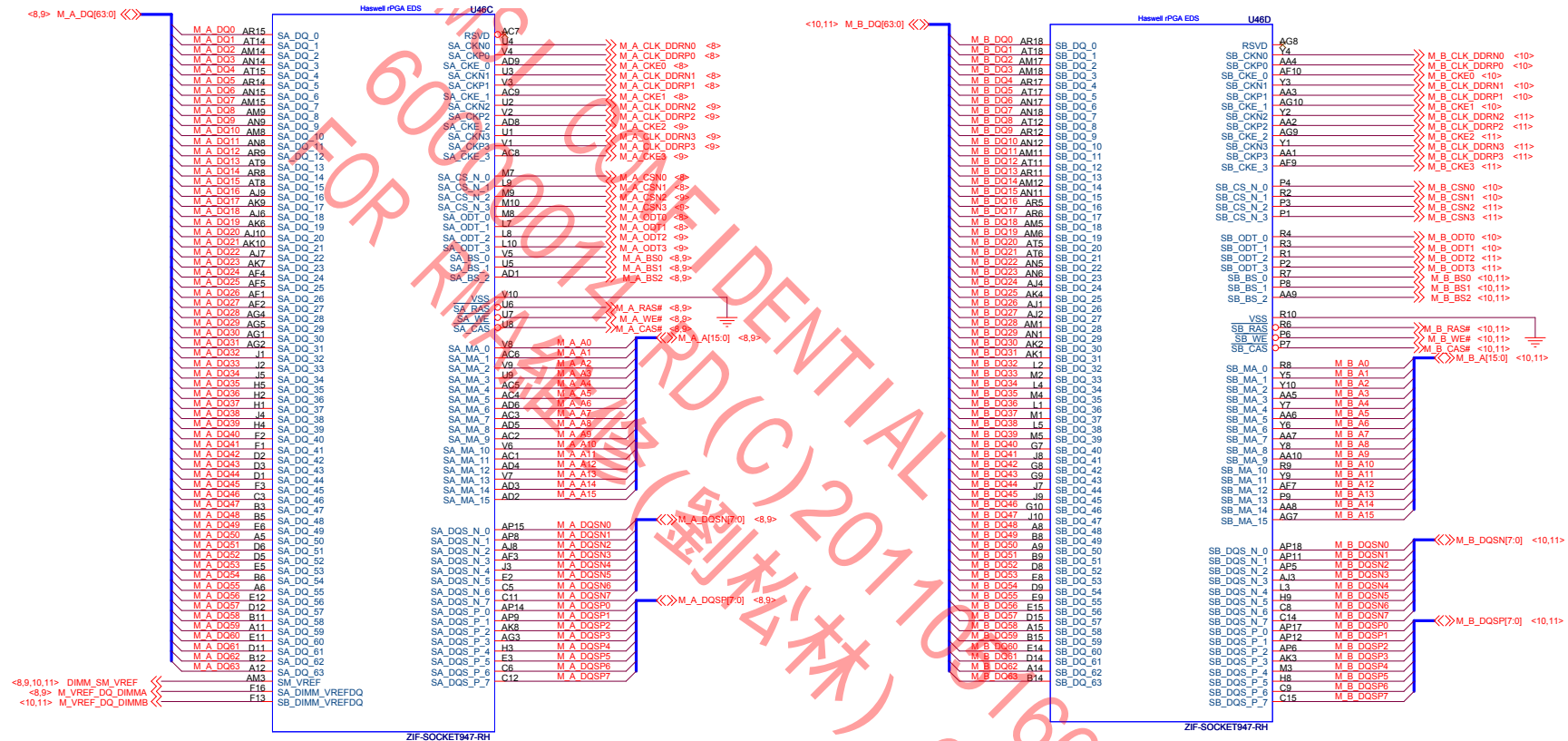
Date	Page	Description	Date	Page	Description	Date	Page	Description
2012.11.20	14	R335 Unstuff						
	20	Change U30 SDA & SCL Pin						
	25	CardReader Change to RTS 5249						
2013.01.14	18	Modify MXM 5VRUN Power						
	19	Modify MXM GC6						
	20	Modify ANX 1122 SMB Channel						
		Ver. Change to 1.0						
2013.01.21	28	PQ13 & PQ14 Change to D03-0444703-A68						
		Ver. Change to 1.1						
2013.03.12		Add LED Function						

MSI CONFIDENTIAL
60000014 RD(C)20110516001
FOR RMA維修(劉松林) ONLY

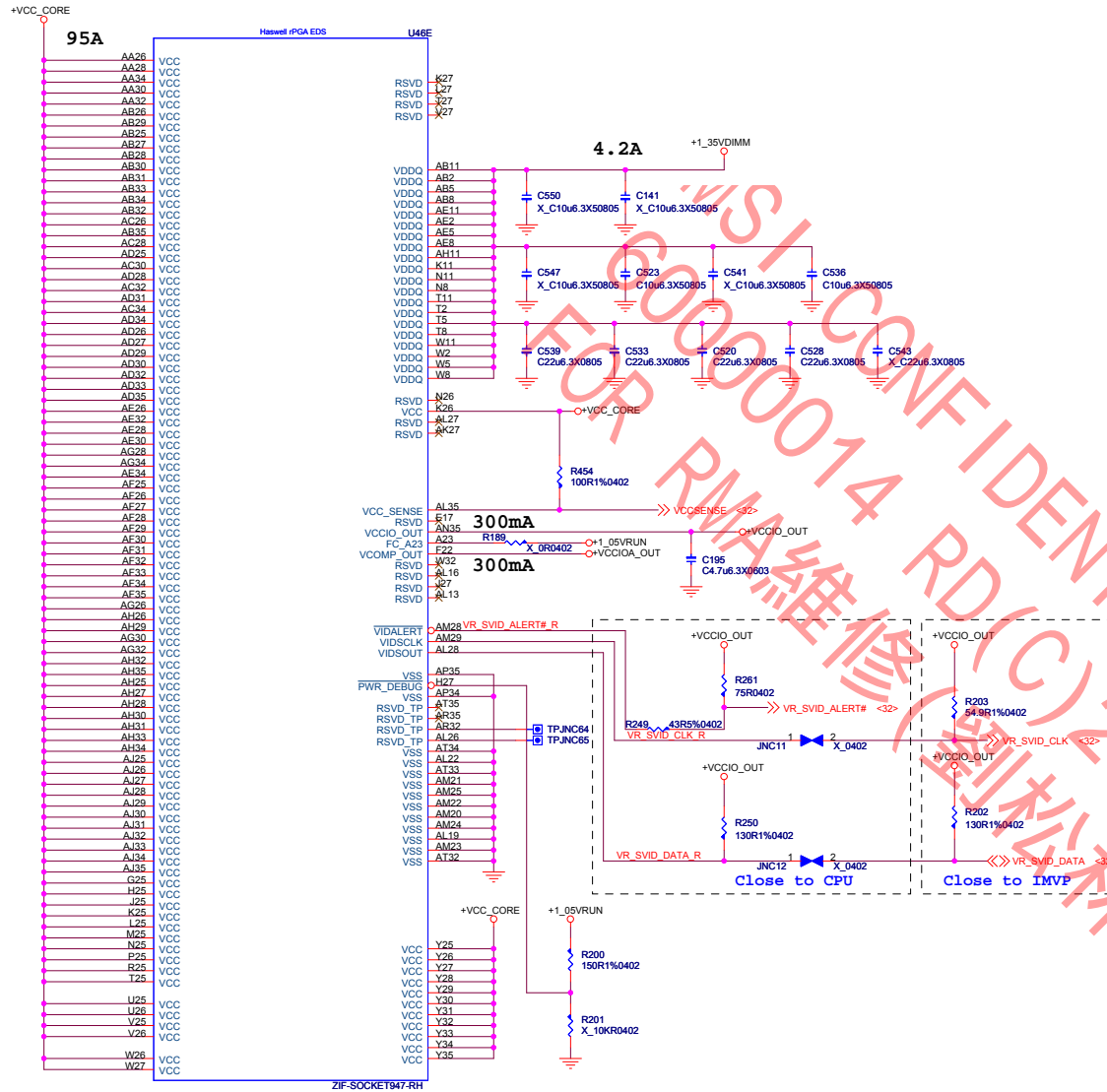
Haswell Processor (DMI,PEG,FDI)

**Haswell Processor (CLK,MISC,JTAG)**

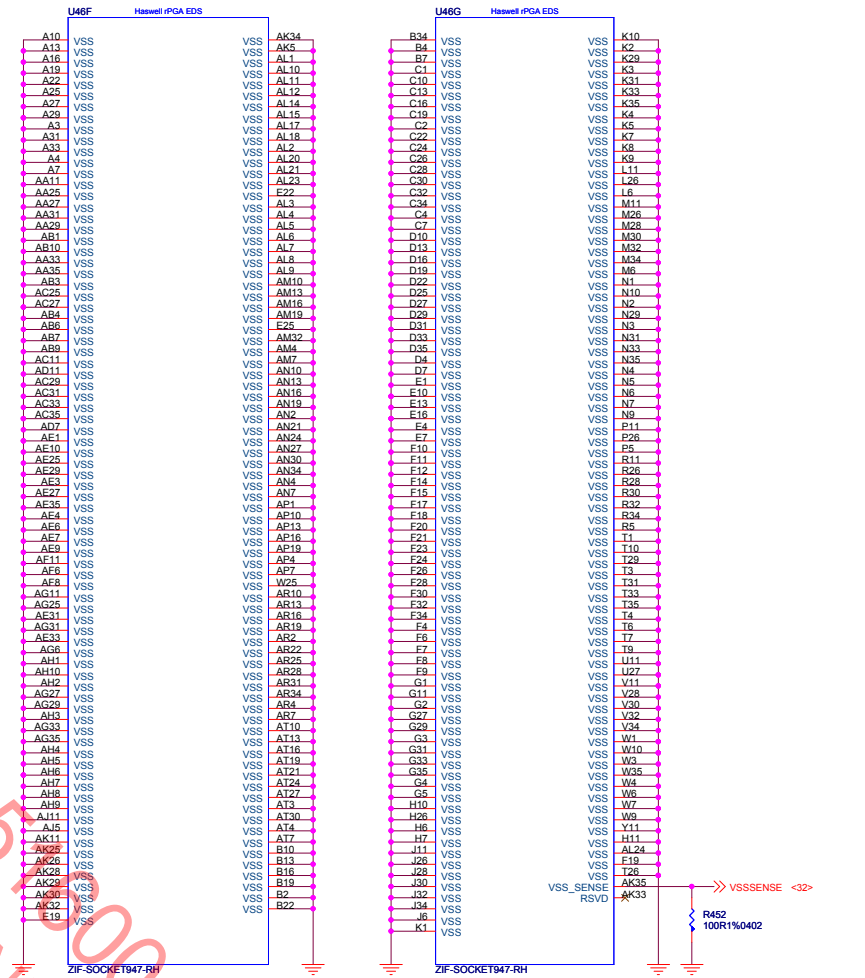
Haswell Processor (DDR3)

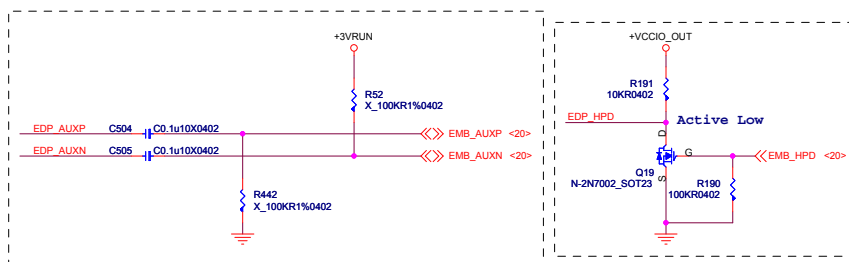
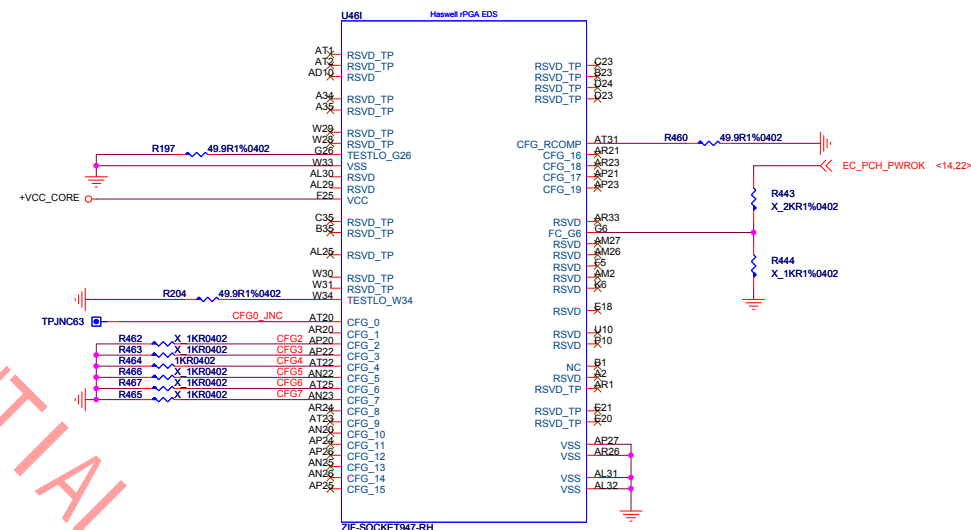


Haswell Processor (Power)



Haswell Processor (Gnd)



Haswell Processor (Reserved)

PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.

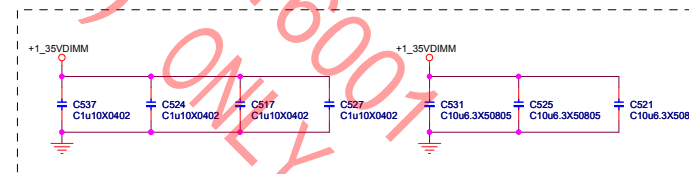
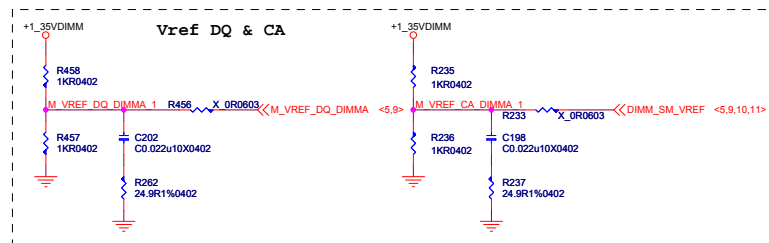
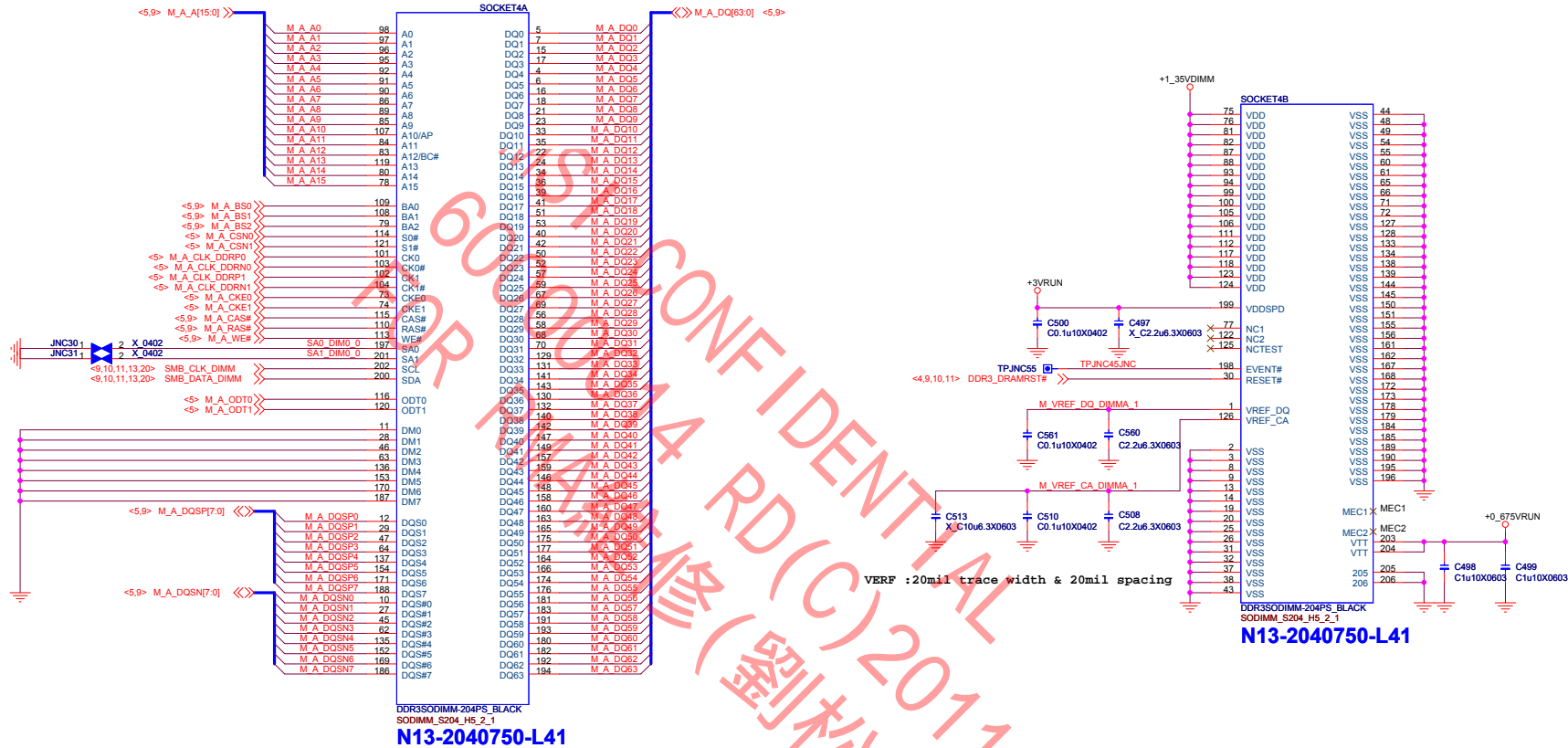
MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

eDP Enable	
CFG4	1 = Disabled 0 = Enabled

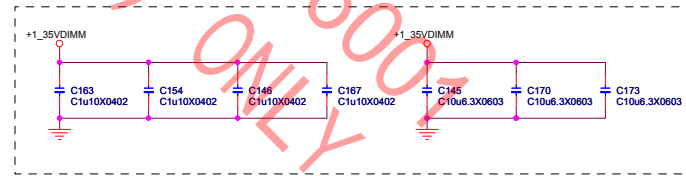
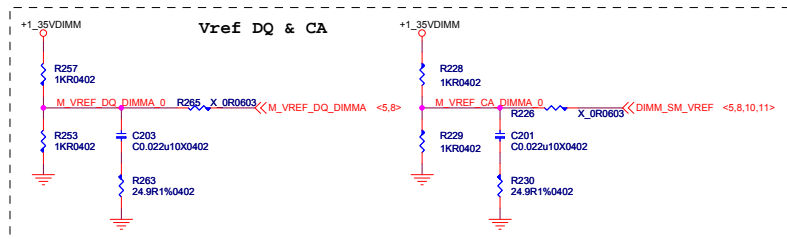
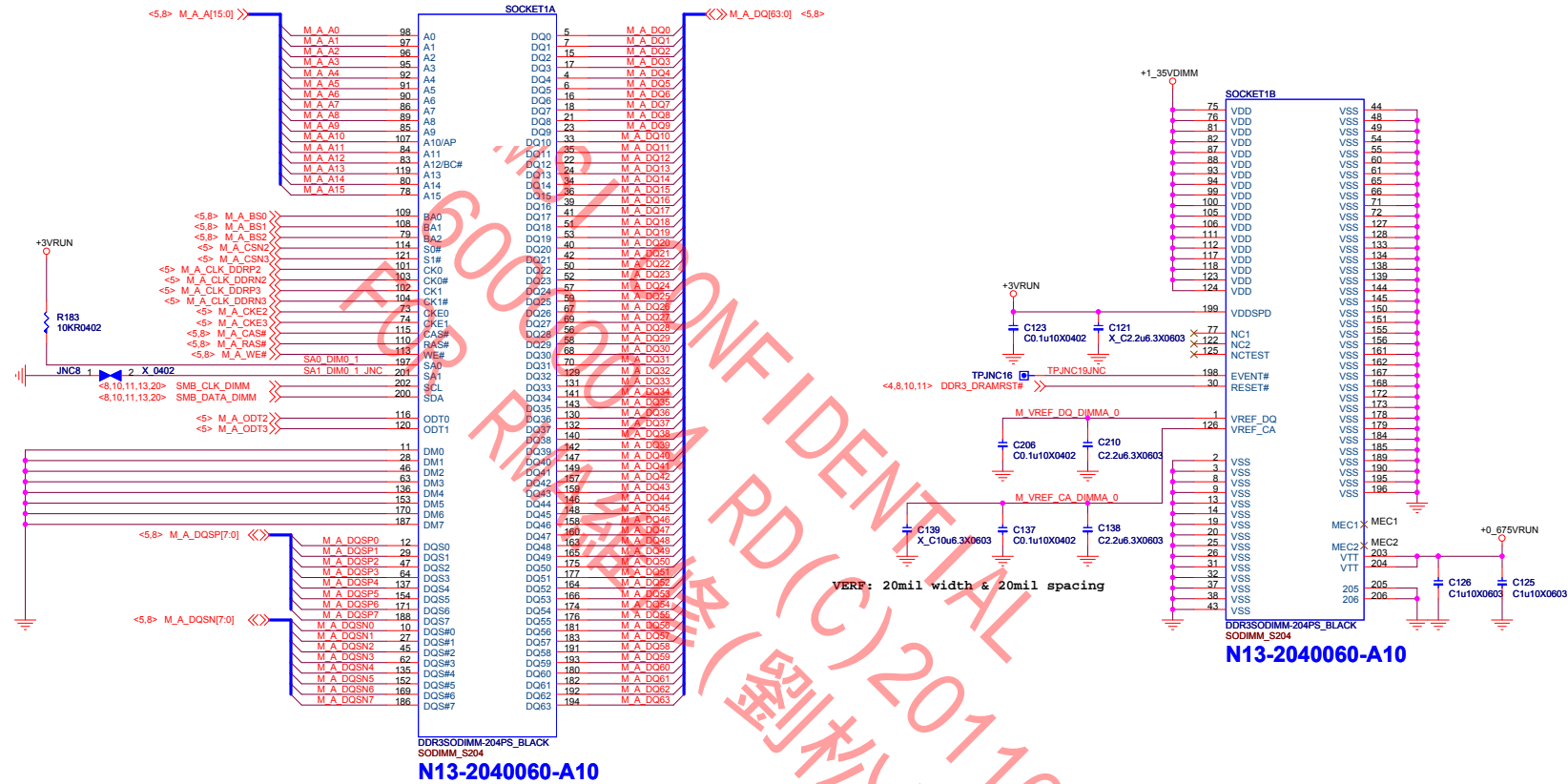
PCI Express* Bifurcation	
CFG[5:6]	00 = 1 x8, 2 x4 PCI Express
	01 = reserved
	10 = 2 x8 PCI Express
	11 = 1 x16 PCI Express

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

SODIMM #A0



SODIMM #A1



VER: 20mil trace width & 20mil spacing

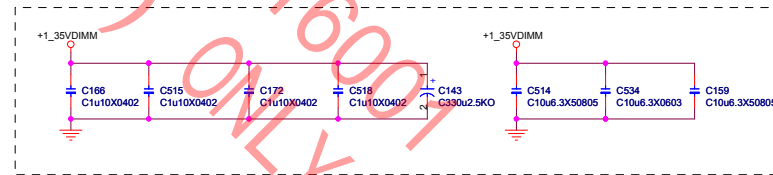
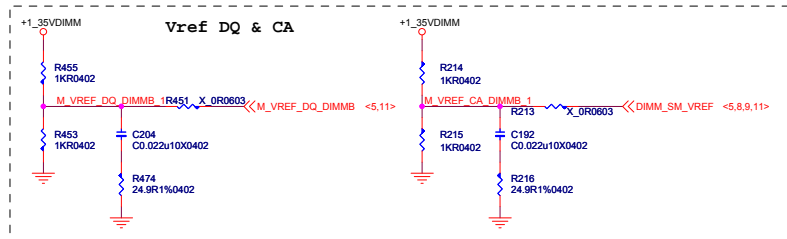
1.35V DIMM

C509 X_C10u6.3X0603 C512 C0.1u10X0402 C507 C2.2u6.3X0603 C518 C1u10X0402

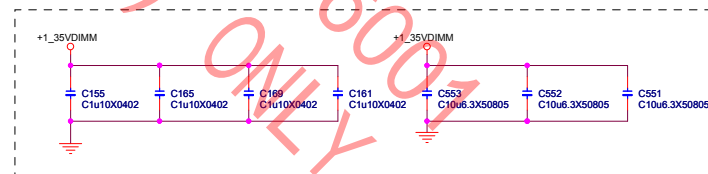
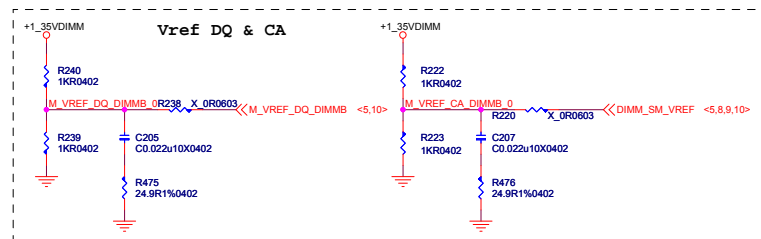
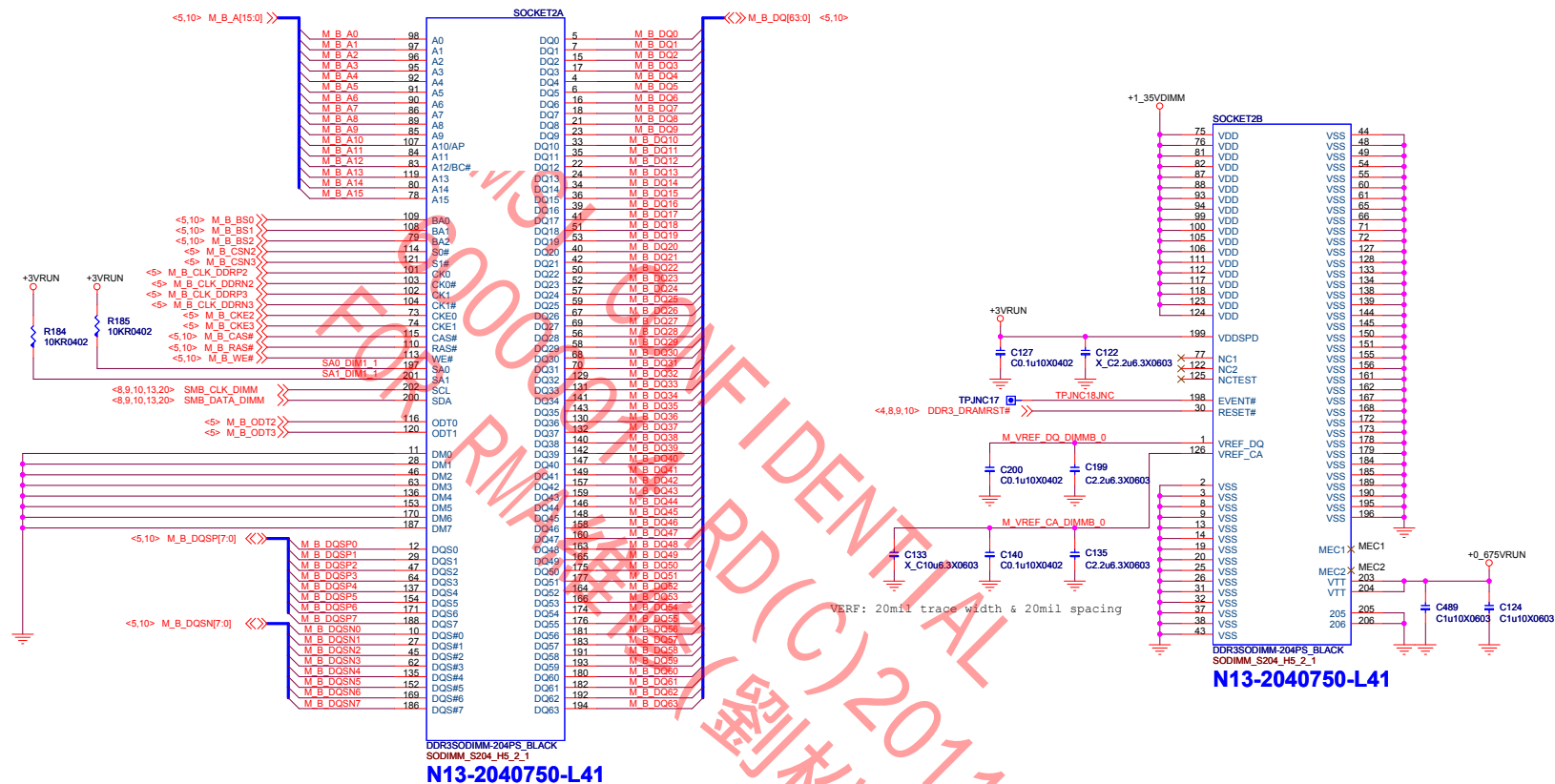
13. VS 14. VS 19. VS 20. VS 25. VS 26. VS 31. VS 32. VS 37. VS 38. VS 43. VS

DFP DFP

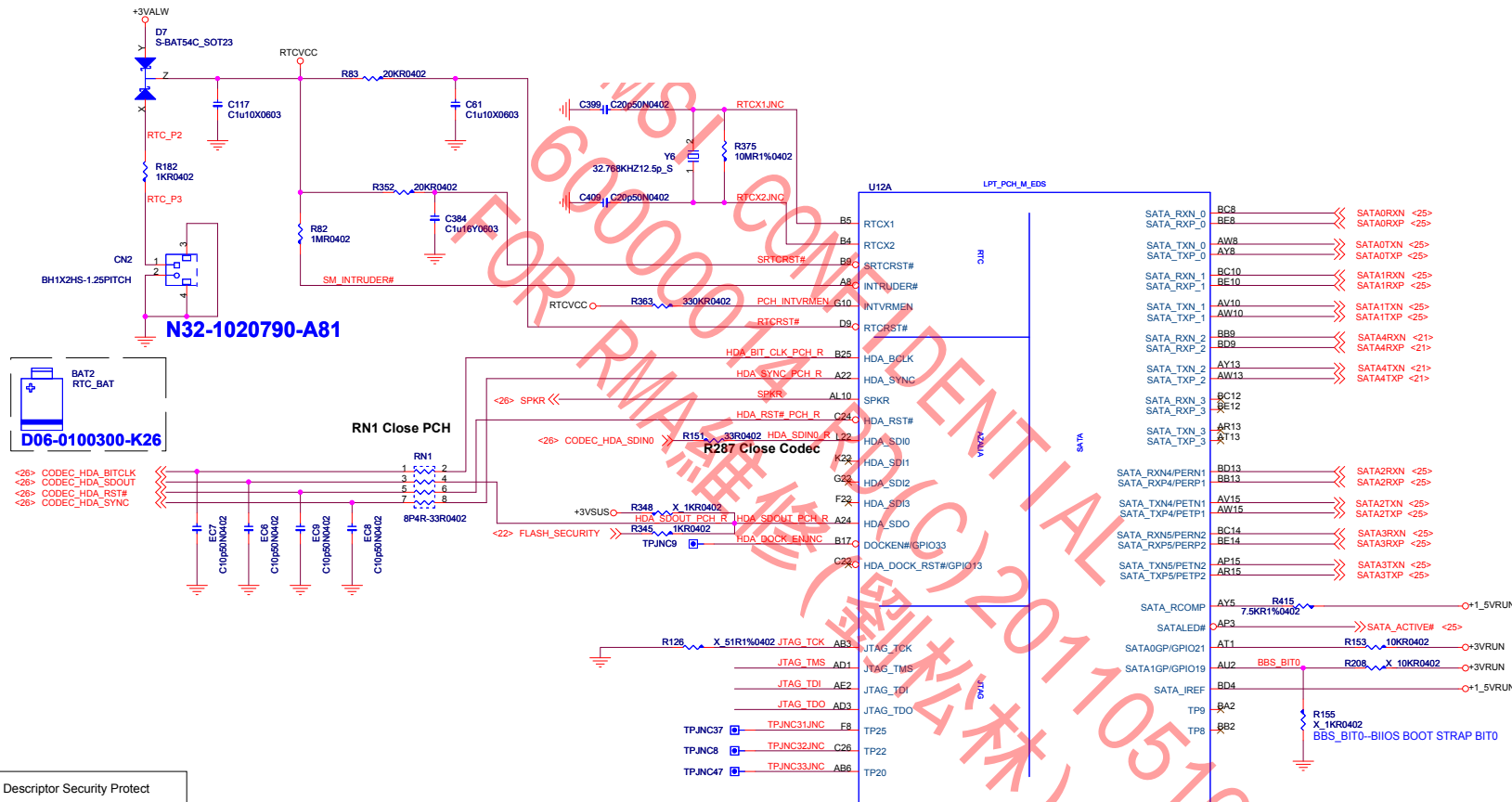
2011051600



SODIMM #B1



Lynx Point (HDA,JTAG,SATA)



SATA	
Port	Device
0	mSATA Gen3(6Gb/s)
1	mSATA Gen3(6Gb/s)
2	ODD(Gen2)
3	NC
4	mSATA Gen3(6Gb/s)
5	To A board(Gen3)

Flash Descriptor Security Protect	
HDA_SDO	Low = Enable High = Disable

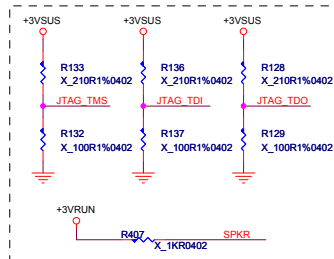
Signal has a weak internal pull-down
Note: The weak internal pull-down is disabled after PLTRST# deasserts.

SPK	The Signal has a weak internal pull-down. Note: the internal pull-down is disabled after PLTRST# deasserts. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature)
-----	--

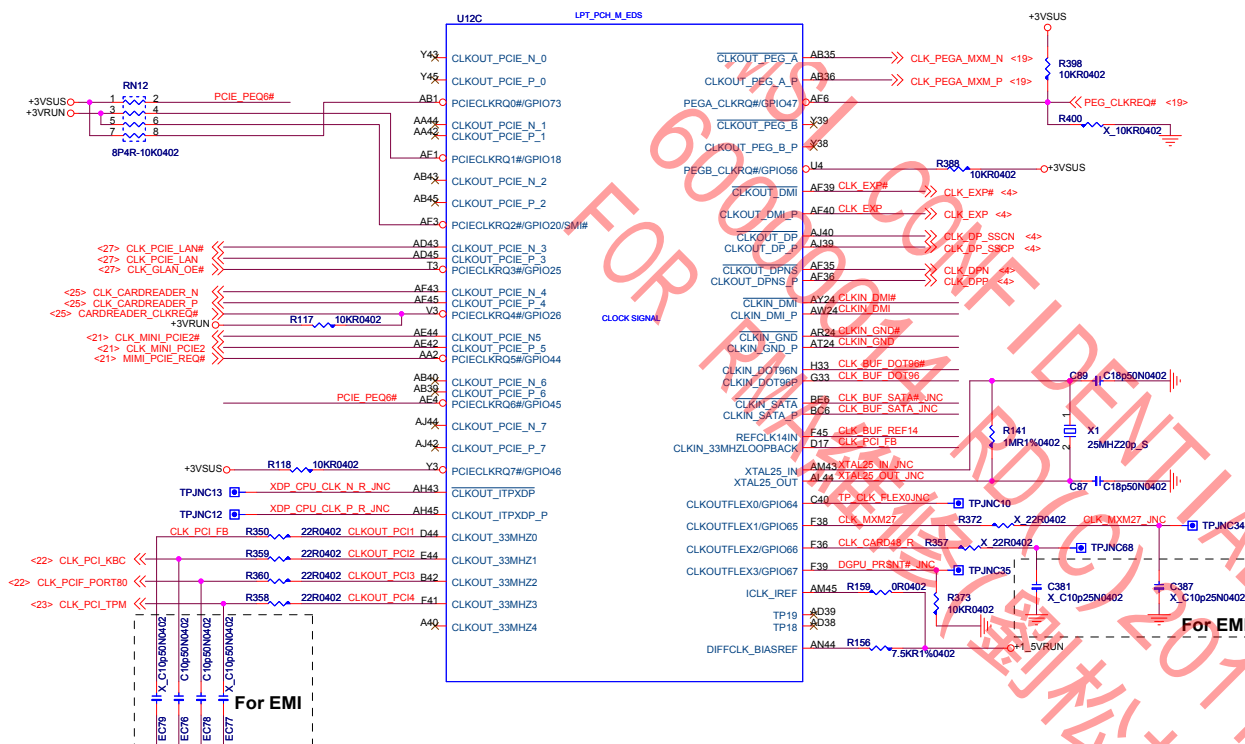
Reserved for Codec use RUN.



HDA_SYNC signal also serves as a strap for selecting VRM voltage to the PCH.
The strap is sampled on the rising edge of RSMRST# signal.
Due to potential leakage on the codec (path to GND), the strap may not be able to achieve the Vihmin at PCH input.
Therefore, platform may need to isolate this signal from the codec during the strap phase. The following example circuits maybe used to achieve this purpose.



Lynx Point (Clock)

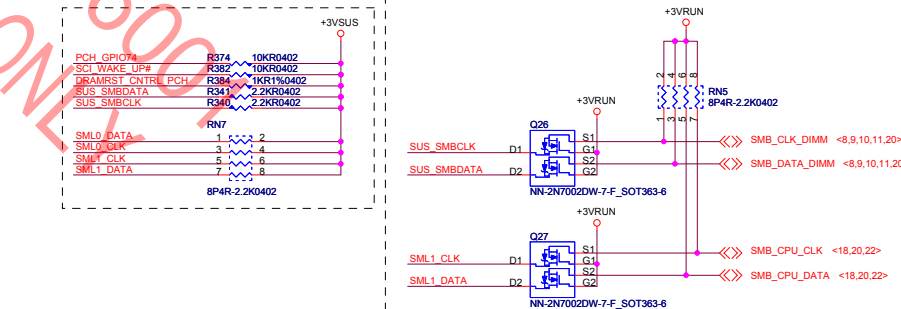
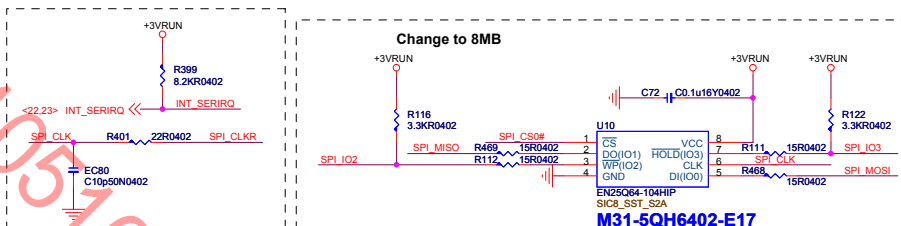
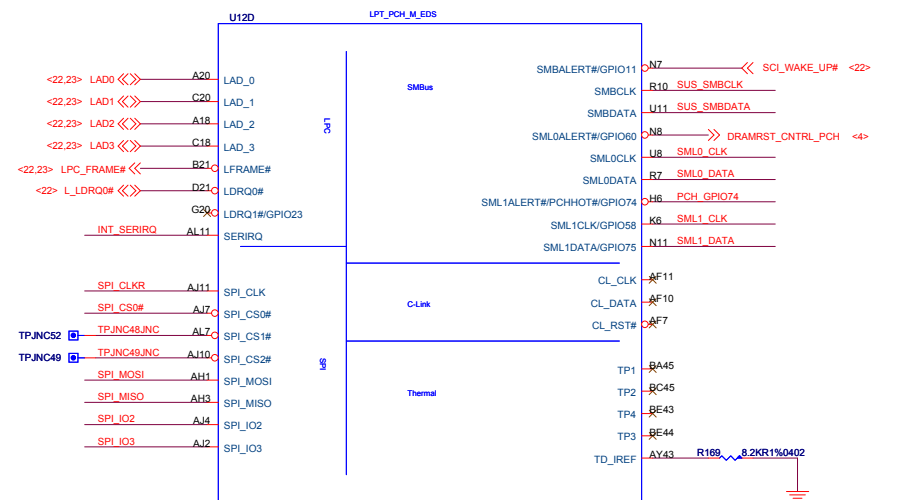


PCIe devices or addin cards that do NOT support CLKREQ# functionality should not route this signal to PCH.
Intel recommends terminating PCIECLKREQ# pin on PCH with 10 kΩ ±10% external pull-up resistor instead of No Connect.
Only PCIECLKREQ[2:1]# on PCH are core well powered. All other PCIECLKREQ# are suspend well powered.

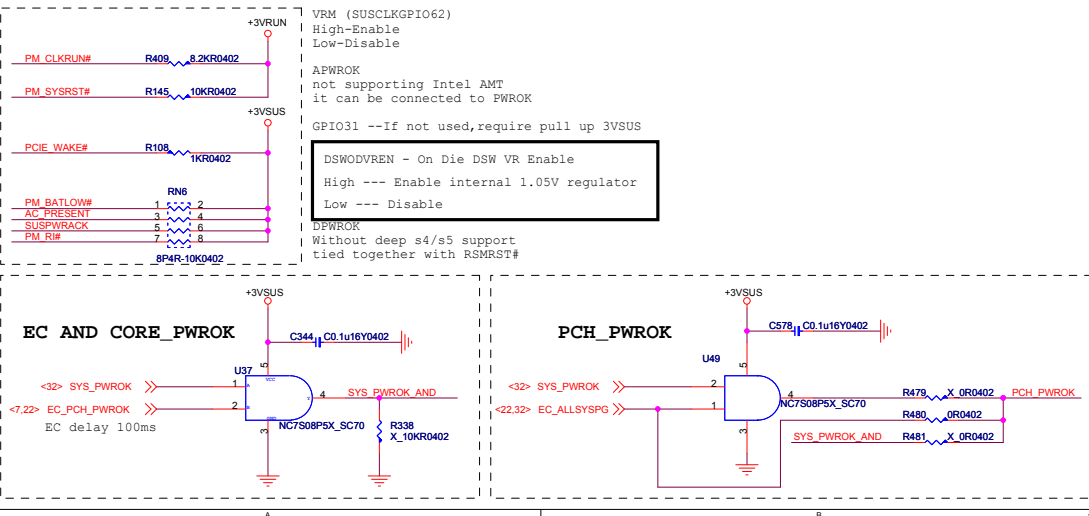
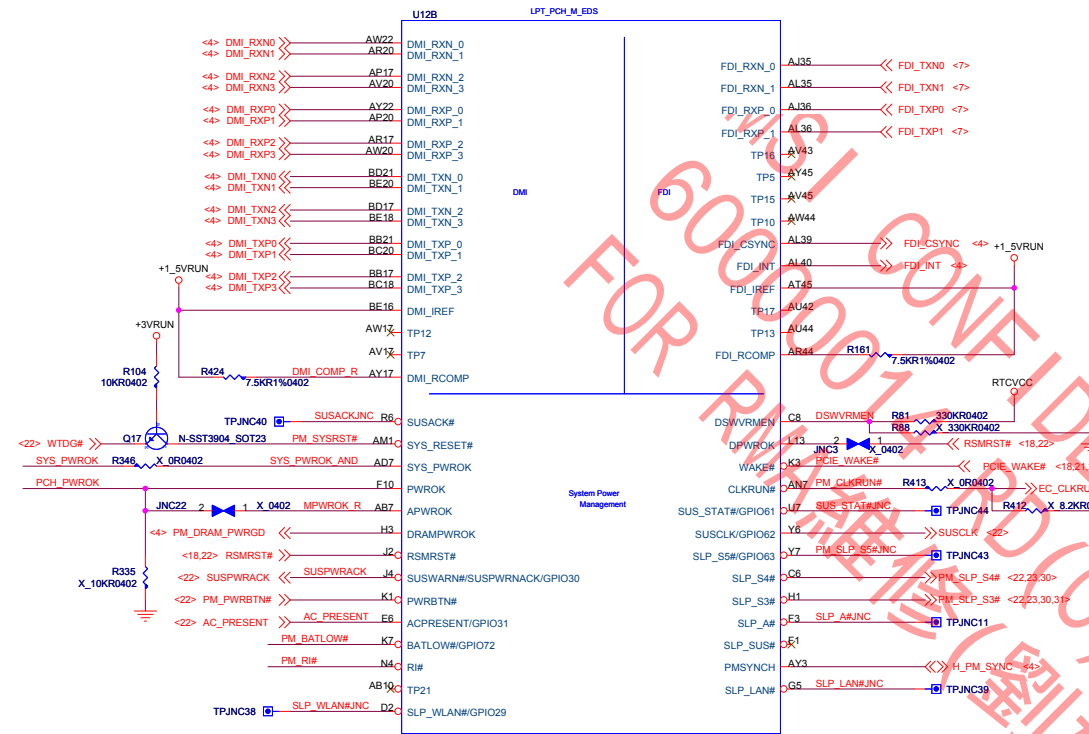
*Disable PCIE OBFF(BIOS)

or Integrated Clock Generation Mode

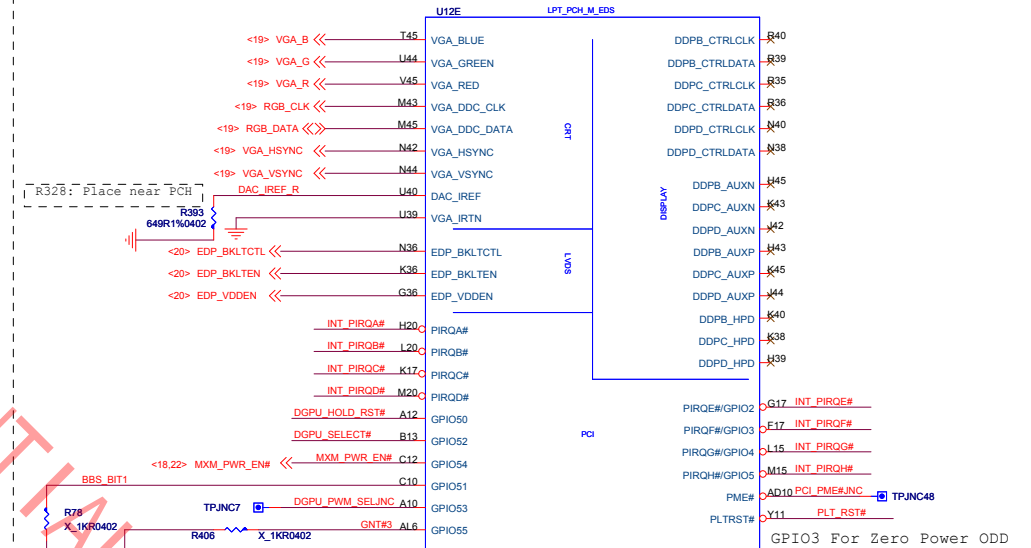
Lynx Point (LPC, SMBUS)



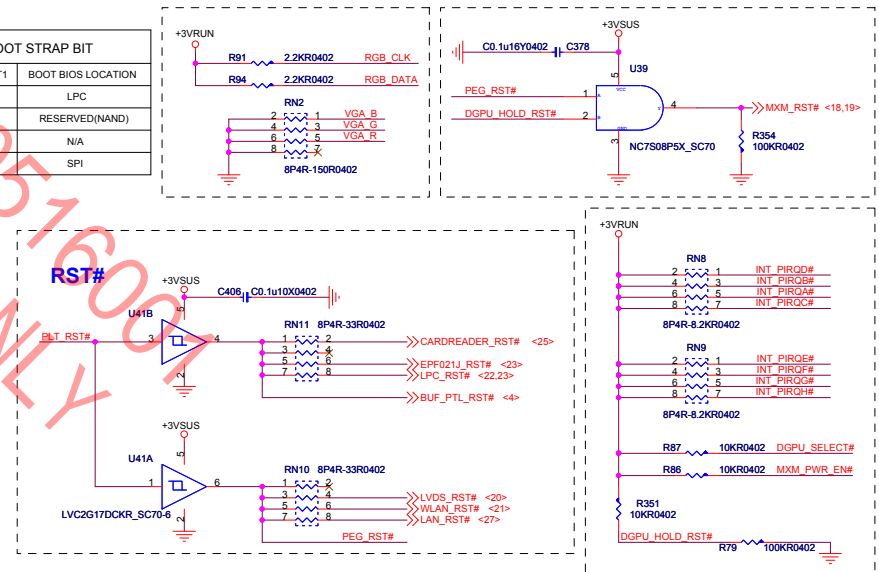
Lynx Point (DMI, FDI)



Lynx Point (PCI, DDI)

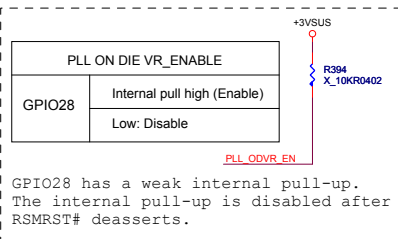
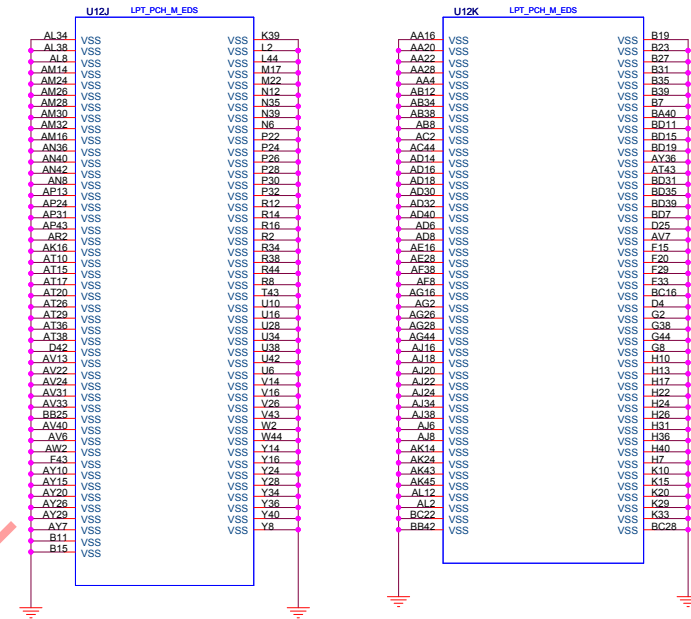
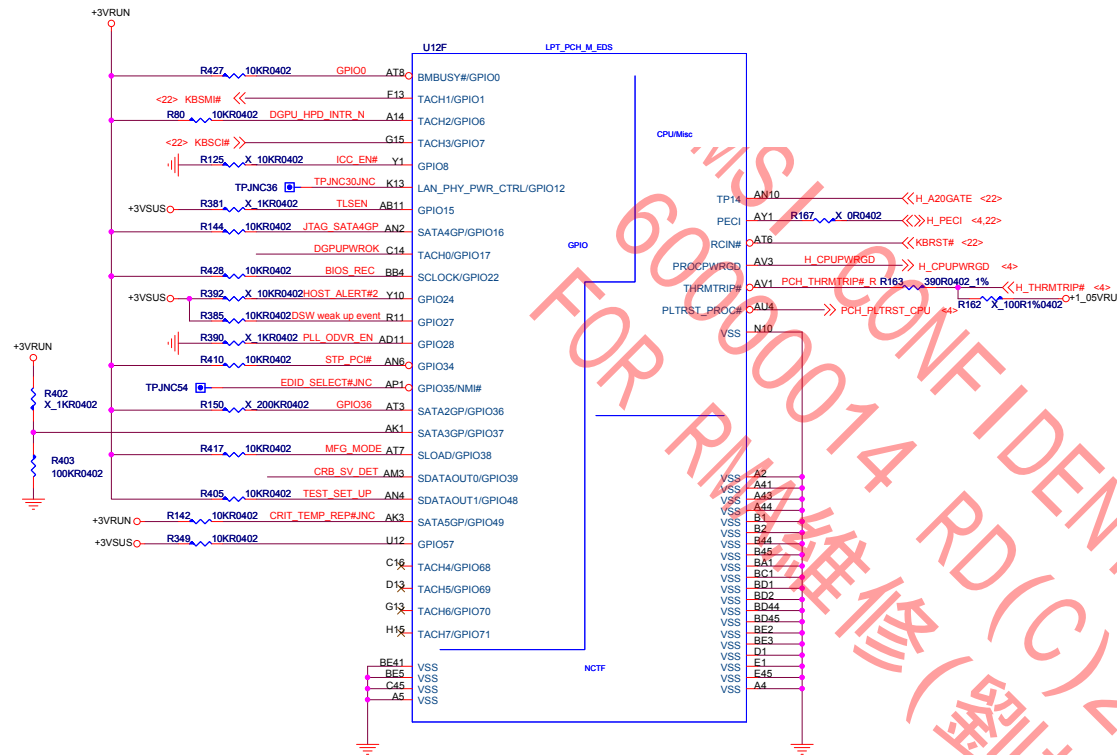


BIOS BOOT STRAP BIT		
BBS_BIT0	BBS_BIT1	BOOT BIOS LOCATION
0	0	LPC
0	1	RESERVED(NAND)
1	0	N/A
1	1	SPI



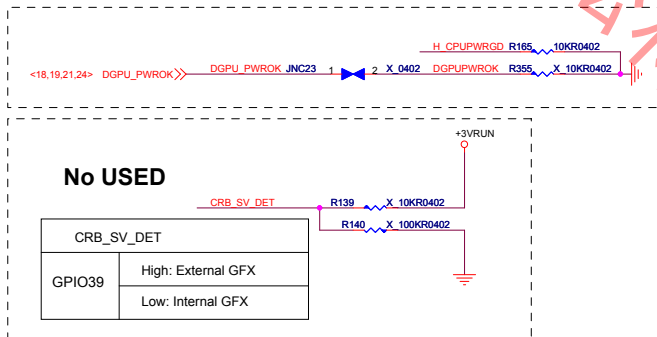
Lynx Point (GPIO,MISC)

Lynx Point (Gnd)



SATA3GP/GPIO37
This signal has a weak internal pull-down.
NOTE:
The internal pull-down is disabled after PLTRST# deasserts.
NOTE:
This signal should not be pulled high when strap is sampled.

This signal has a weak internal pull-down.
NOTE:
The internal pull-down is disabled after PLTRST# deasserts.
GPIO36 --CRB connector to 3V

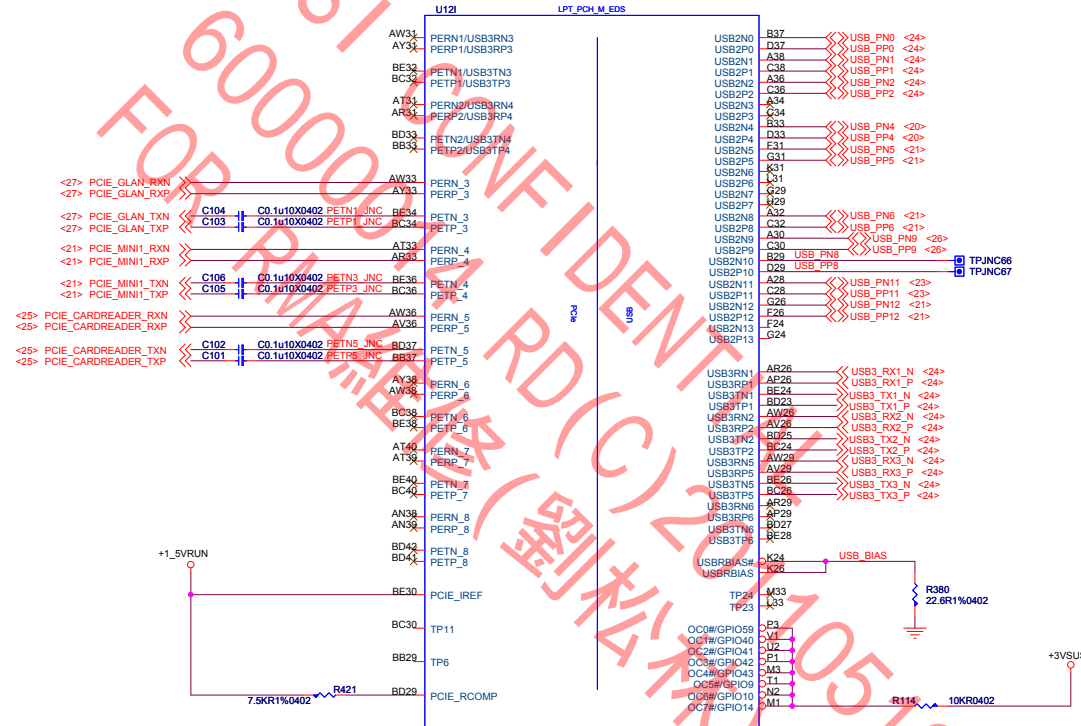


GPIO0 & 6 & 16 & 17 & 22 & 34 & 38 & 48 --If not used,require pull up 3VRUN
GPIO57 --If not used,require pull up 3VSUS
GPIO15--Not support AMT,Transport Layer Security Disable(High is support TLS,internal pull-down)
GPIO27 is deep S4 & S5 weak up event,internal pull high.& It's VCCFDIPLL internal VRM strapping pin
GPIO35 --Define to EDID Select (If not used,require pull down)

SATA2GP/GPIO36 (net name: FDI_OVRVLTG) & SATA3GP/GPIO37 (net name: SATA_ODD_PRSTNT#)
Sampled at Rising edge of PWROK.
Weak internal pull-down. (weak internal pull-down is disabled after PLTRST# de-asserts)
NOTE: This signal should NOT be pulled high when strap is sampled

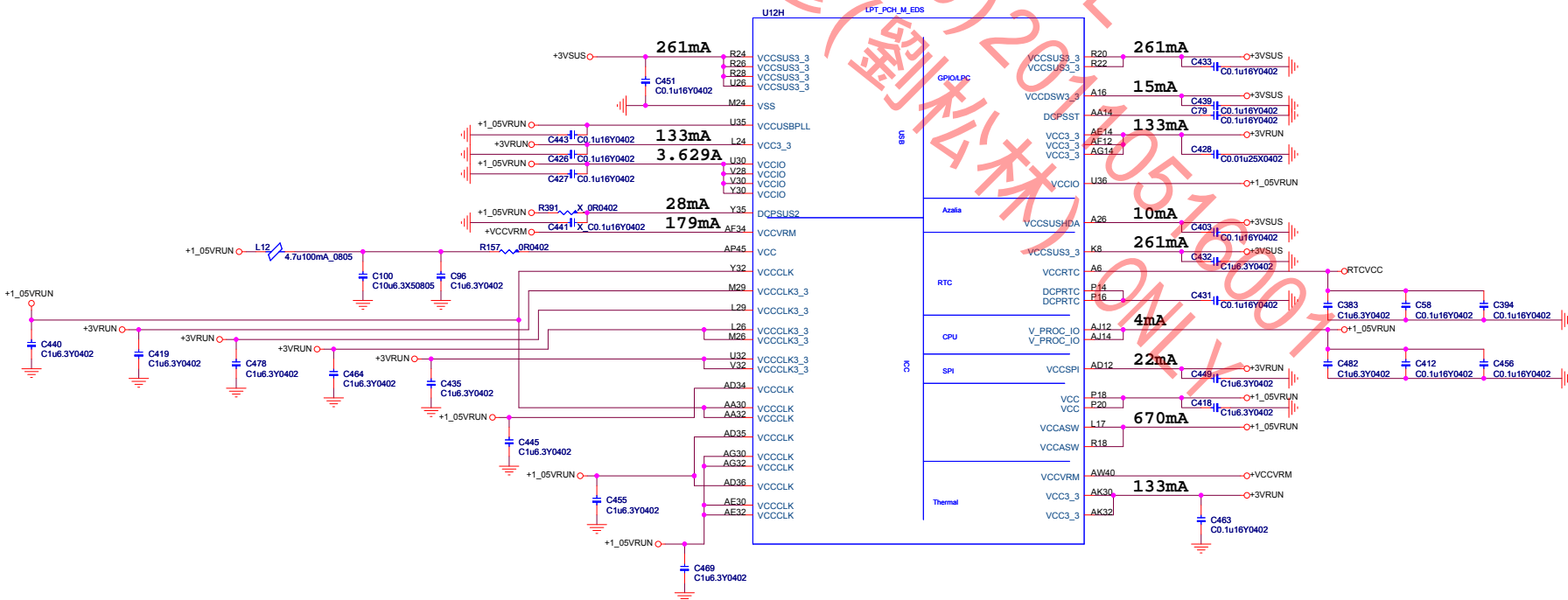
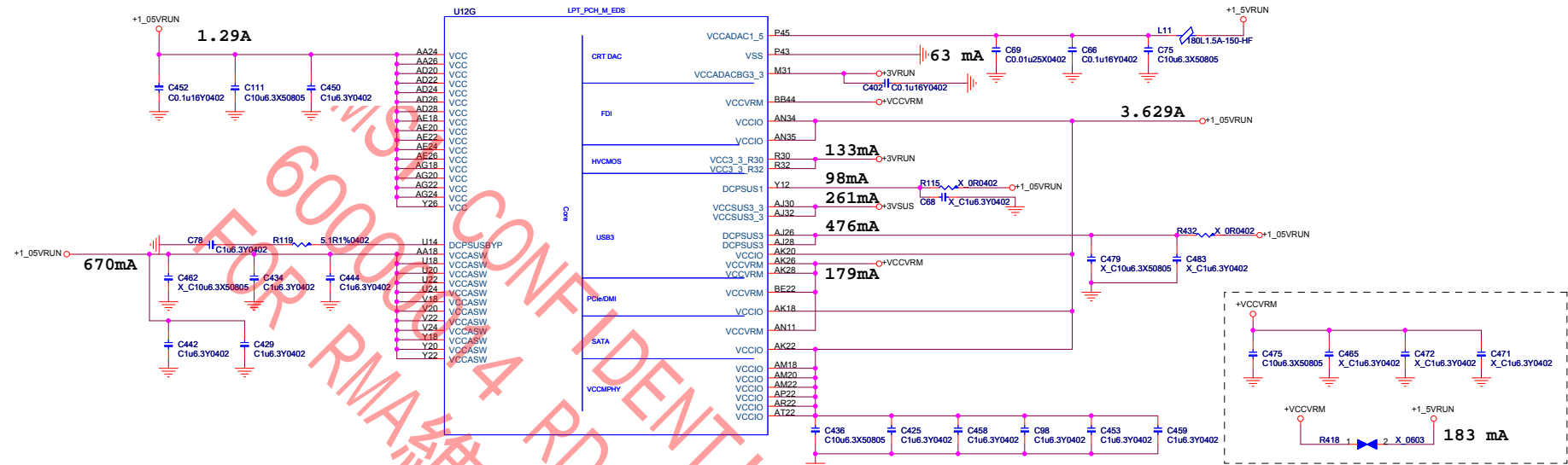
Lynx Point (PCIE,USB)

PCI-E	
Port	Device
3	Giga Lan
4	Mini PCIE-WLAN
5	Card Reader



USB			
USB 2.0	USB 3.0	Device	Note
0	1	USB 3.0 Port 1	
1	2	USB 3.0 Port 2	Debug Port
2	5	USB 3.0 Port 3	
3			NC
4		WebCam (LVDS)	
5		USB 2.0 Port 5 (1763)	
6			NC
7			NC
8		USB 2.0 Port 5 (1763)	
9		USB 2.0 Port 5 (16F4)	Debug Port
10		TestPad	
11		EPF LED (8051)	
12		Mini PCIE-BT	
13			NC
	3		NC
	4		NC
	6		NC

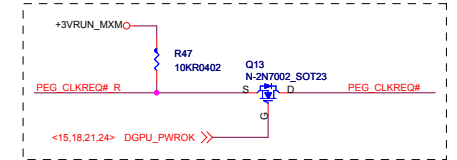
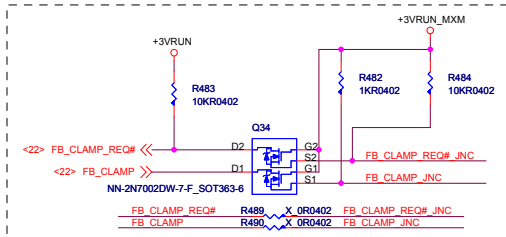
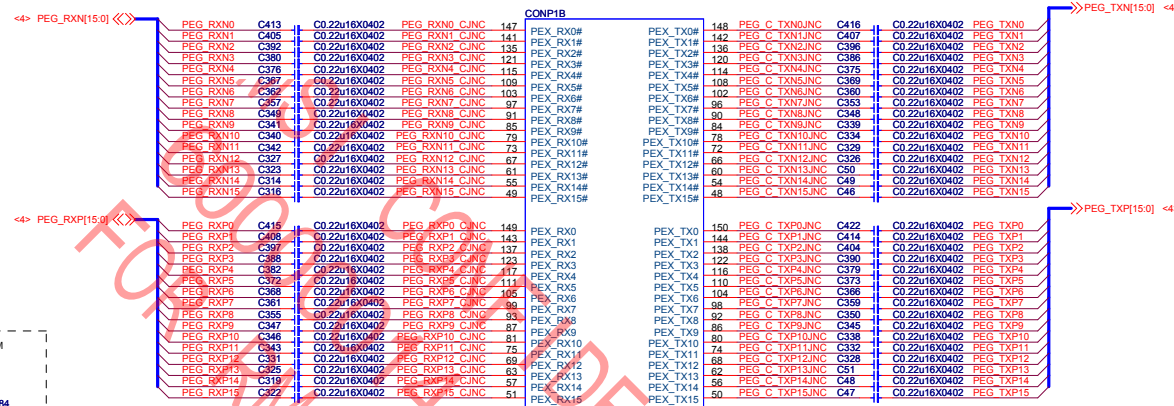
Lynx Point (Power)



MXM 3.0 (x16 PEG Gen 3)

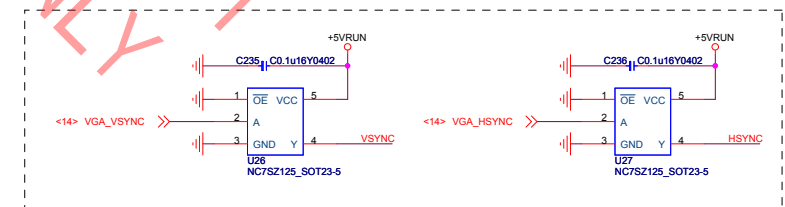
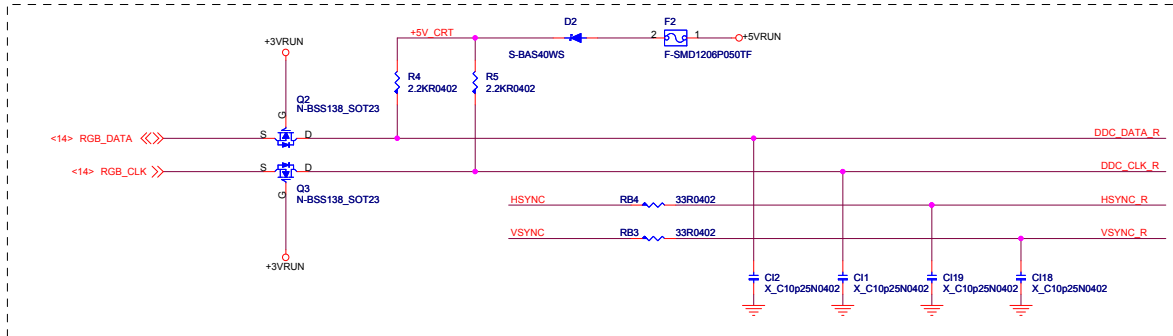
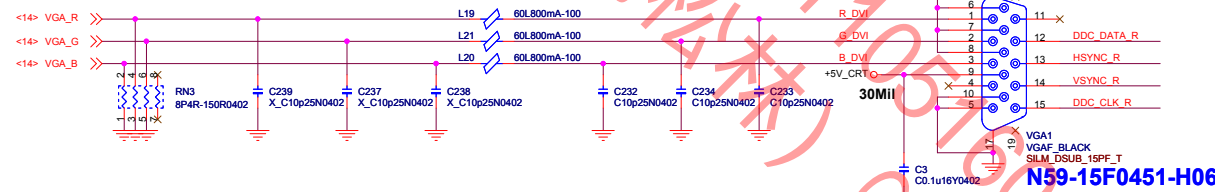
n'VIDIA Comments: NV11 can't support PCIe GEN3,so used 0.1uf CAP

The change in AC capacitor value from 0.1uf to 0.22uf is to enable compatibility with futrue platforms having PCIe GEN3(8GT/s)

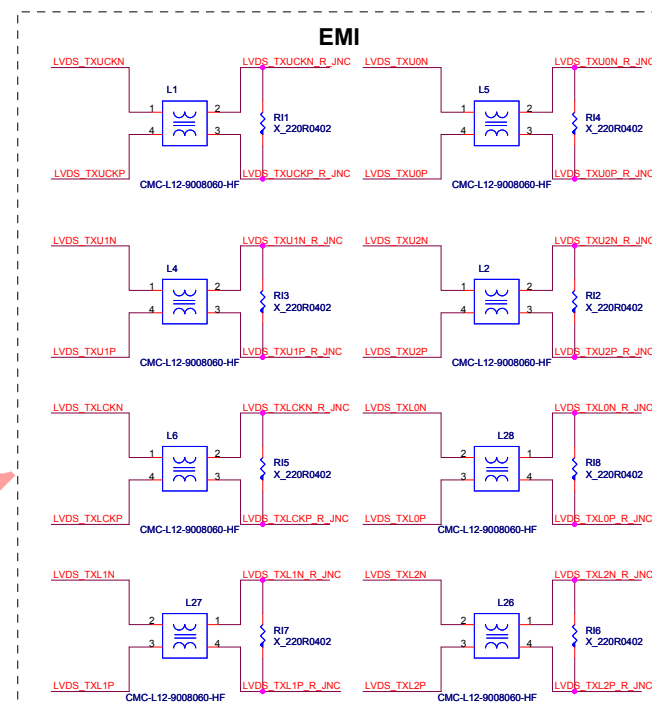
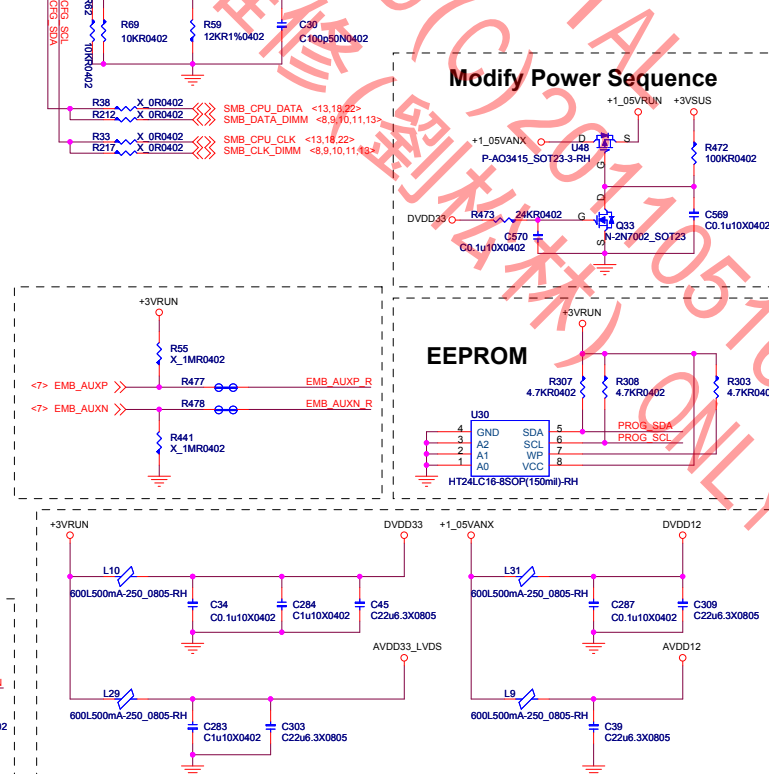
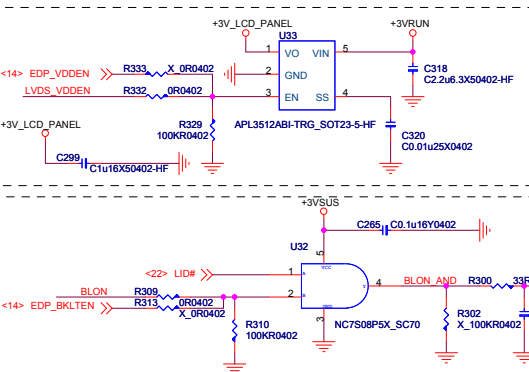
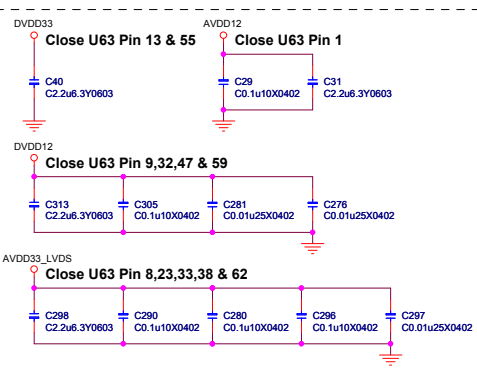
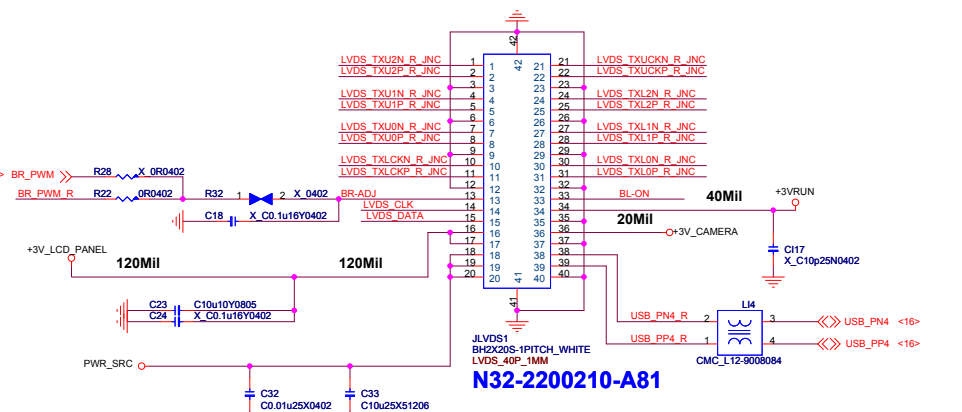
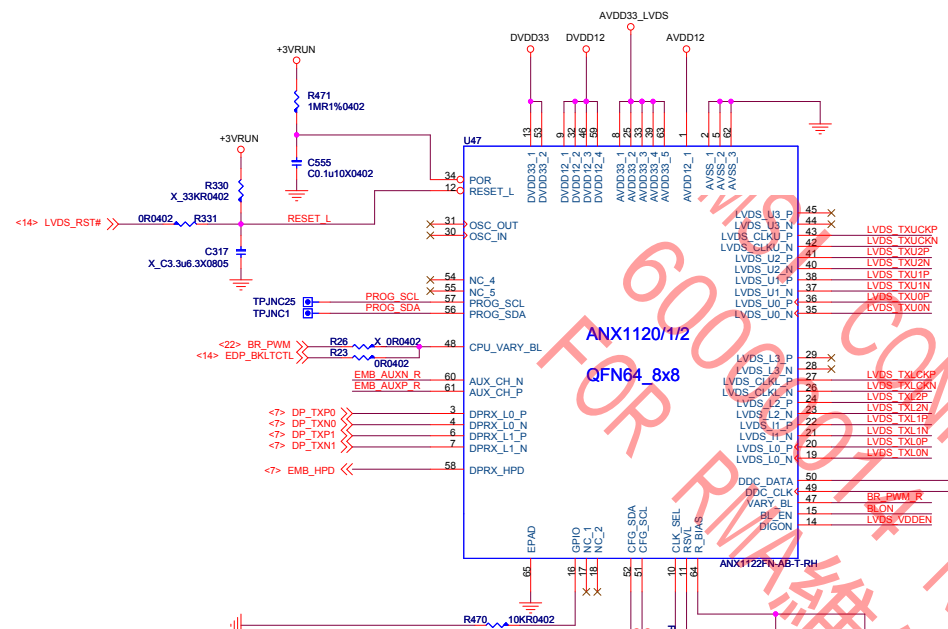


N11-3140030-A81

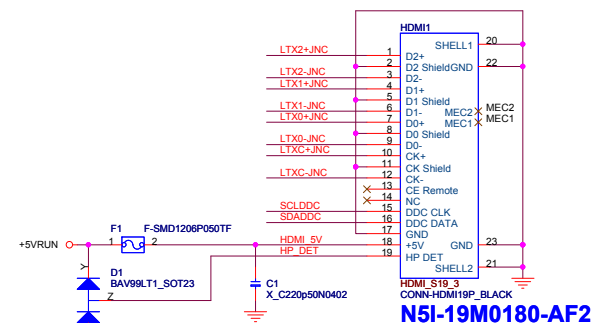
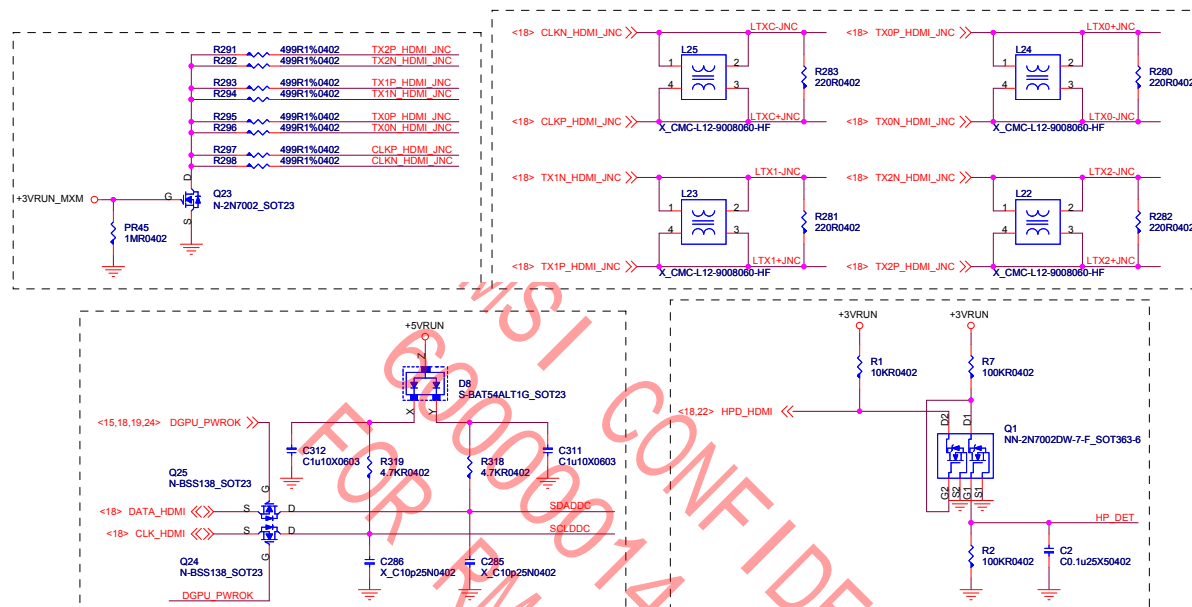
CRT



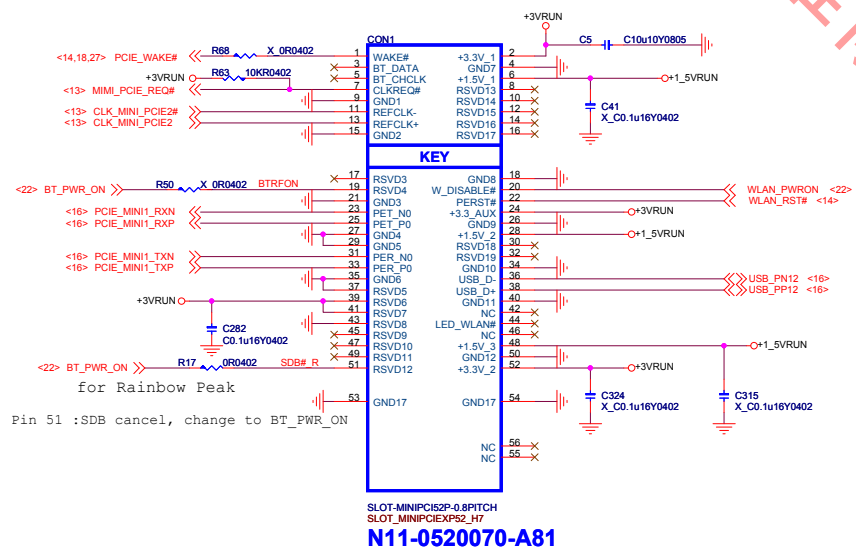
eDP to LVDS



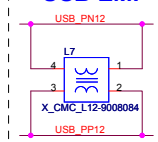
HDMI



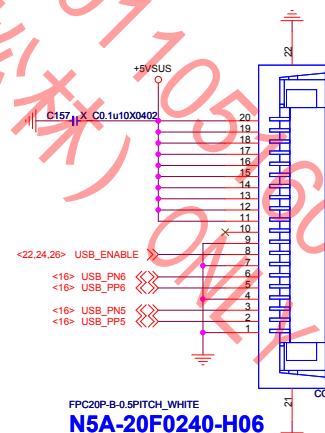
WLAN/BT



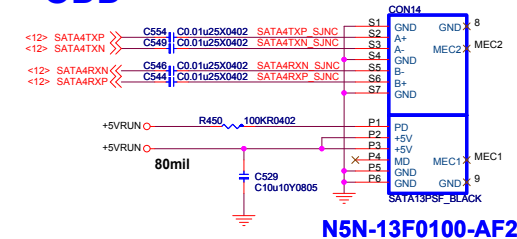
USB EMI



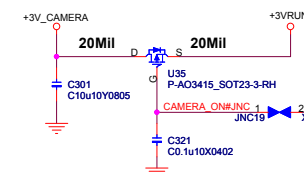
**MS-1763 Co-Lay
USB Port *2**



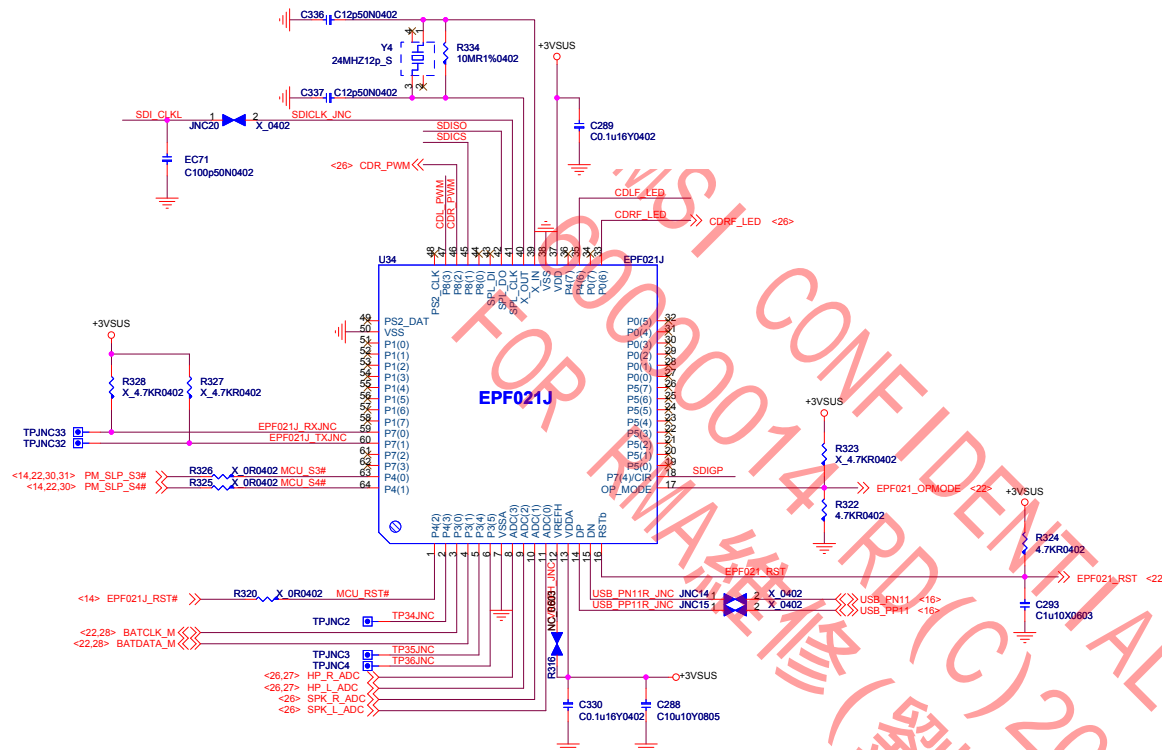
ODD



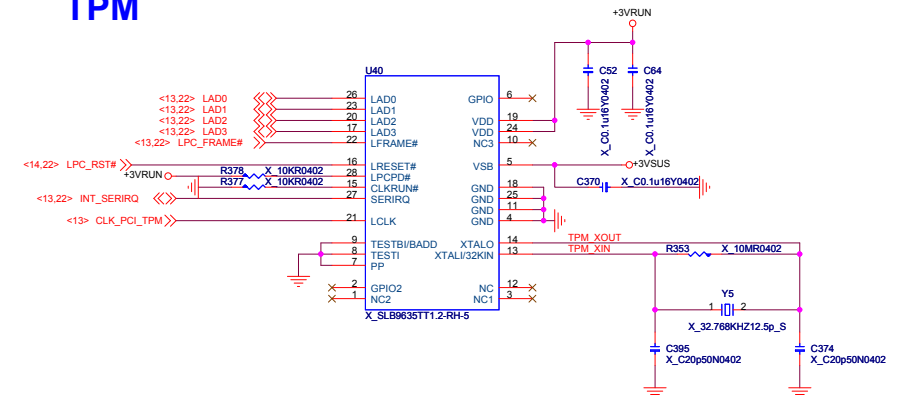
WebCAM



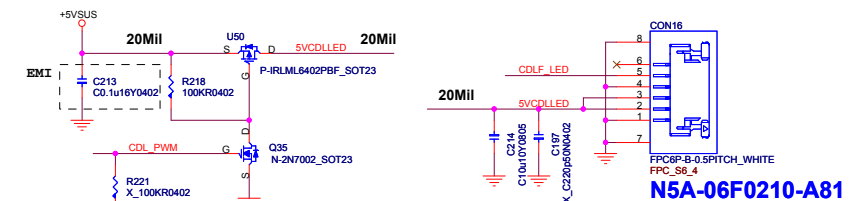
LED 8051 Controller(EPF021J)



TPM



CD_L LED Control

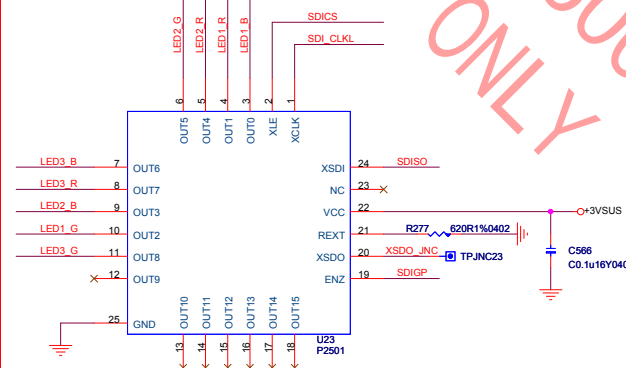
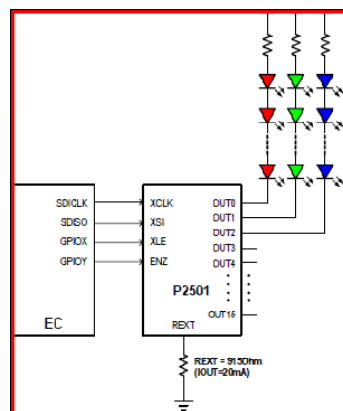


LED Driver IC

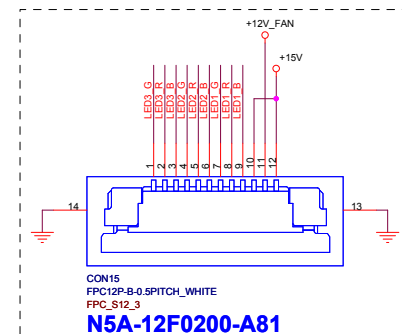
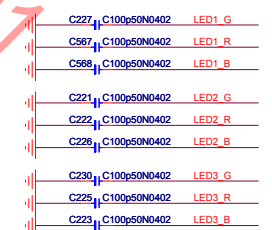
LED Forward Voltage	
R_Max	2.4V x 4 pcs = 9.6V
G_Max	3.3V x 4 pcs = 13.2V
B_Max	3.3V x 4 pcs = 13.2V

Constant current programming through the R258 resistor		
REXT		$I_{OUT} = (V_{REXT} / R_{EXT}) \times 15$ 30mA = $(1.22 / 620) \times 15$
BR1	BR0	Average_1 OUT (ON/OFF)
0	0	3.75mA
0	1	11.25mA
1	0	18.75mA
1	1	26.25mA

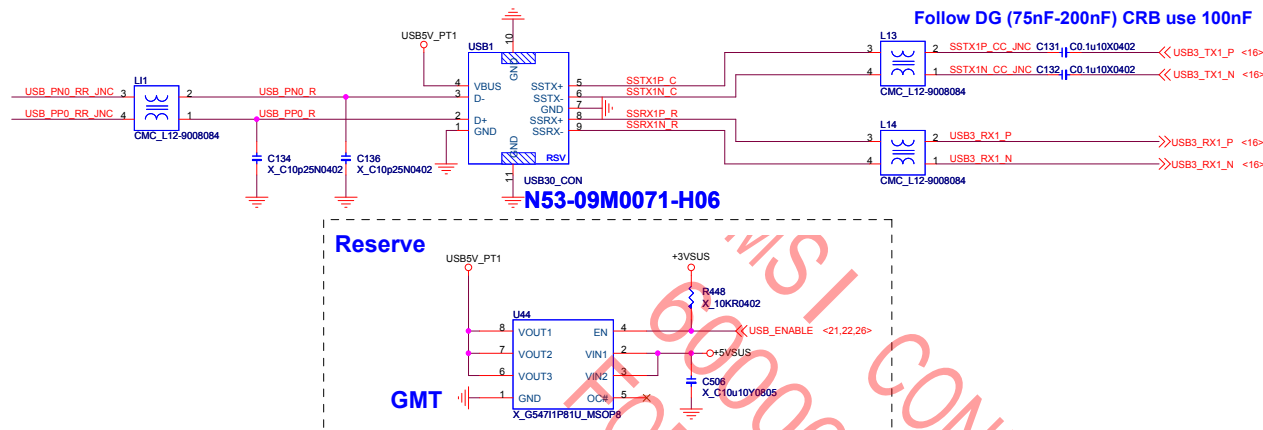
LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G



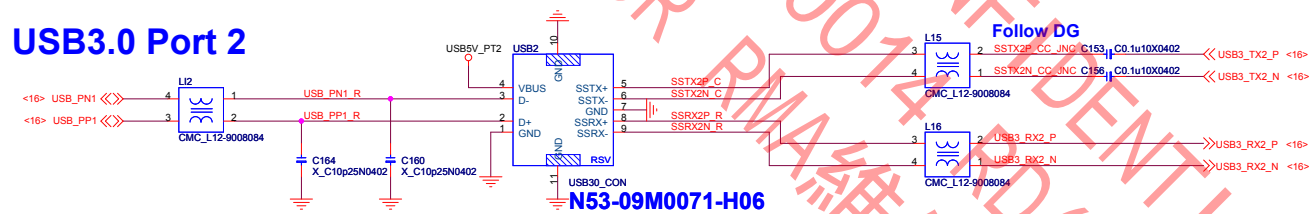
For EM



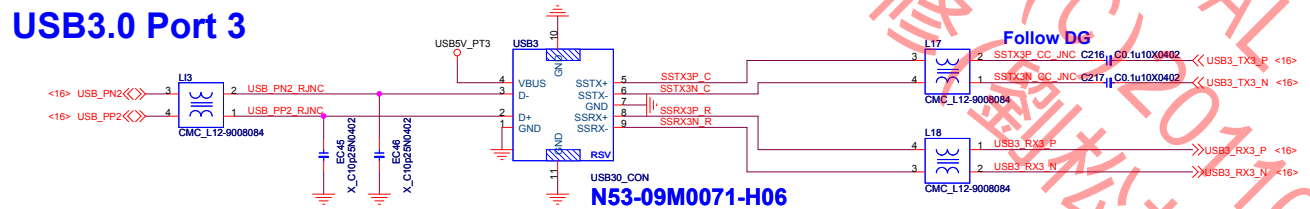
USB3.0 Port 1



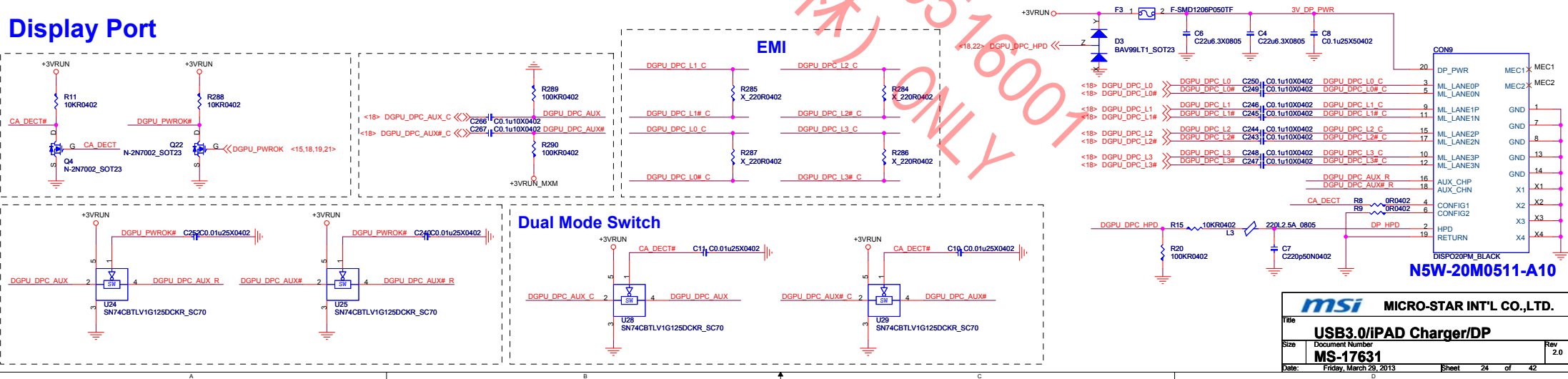
USB3.0 Port 2



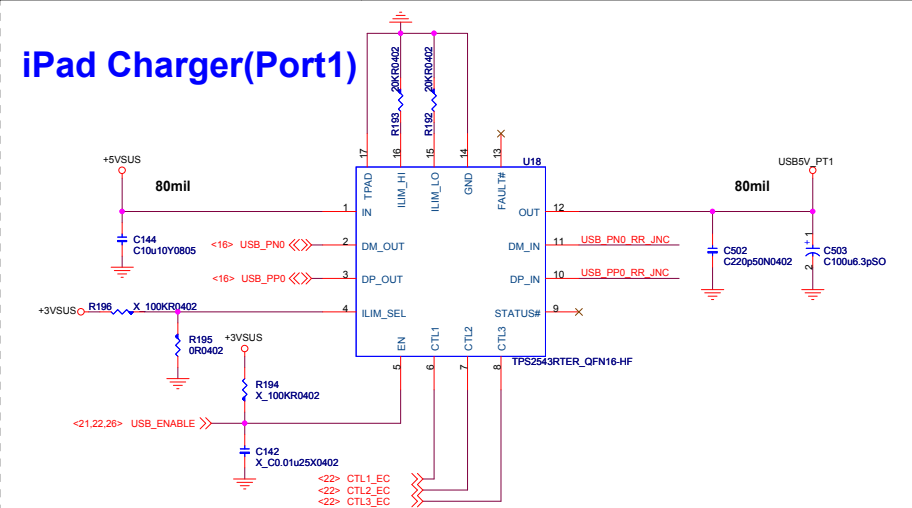
USB3.0 Port 3



Display Port



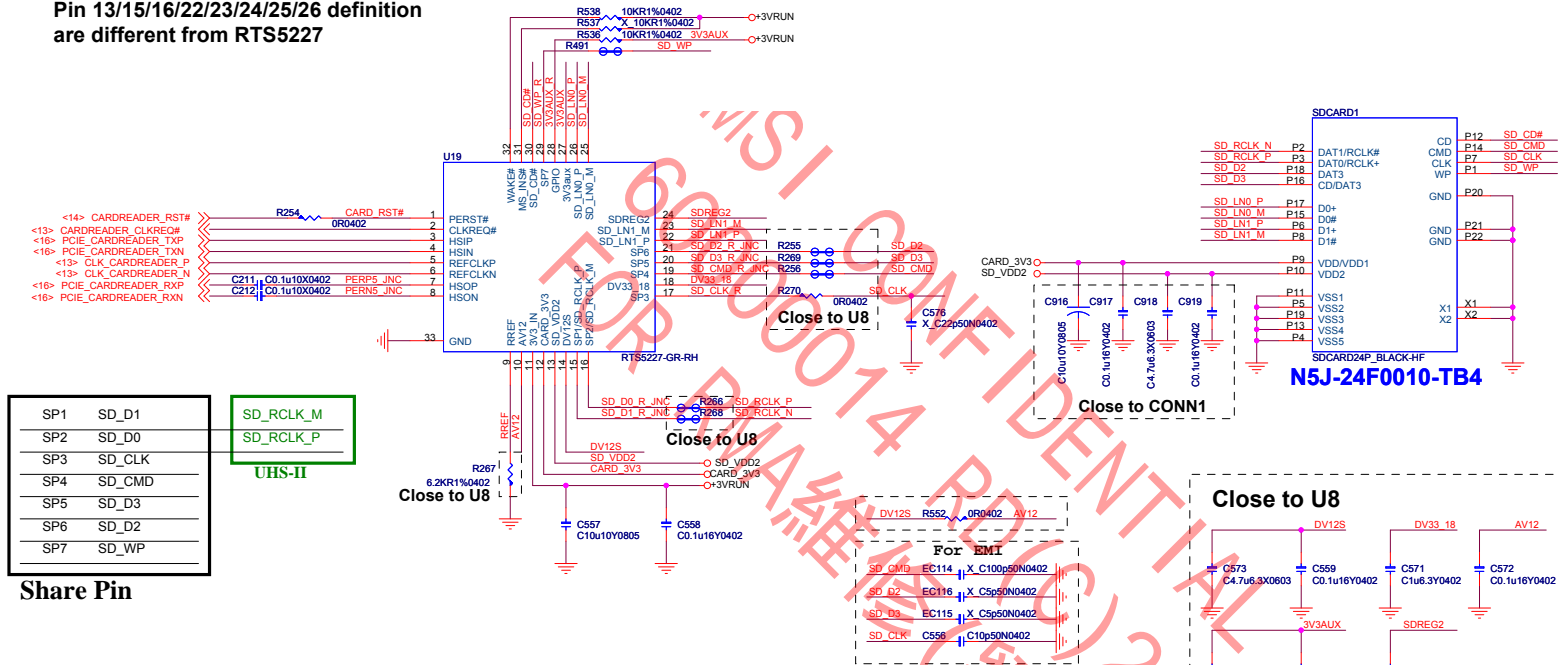
iPad Charger(Port1)



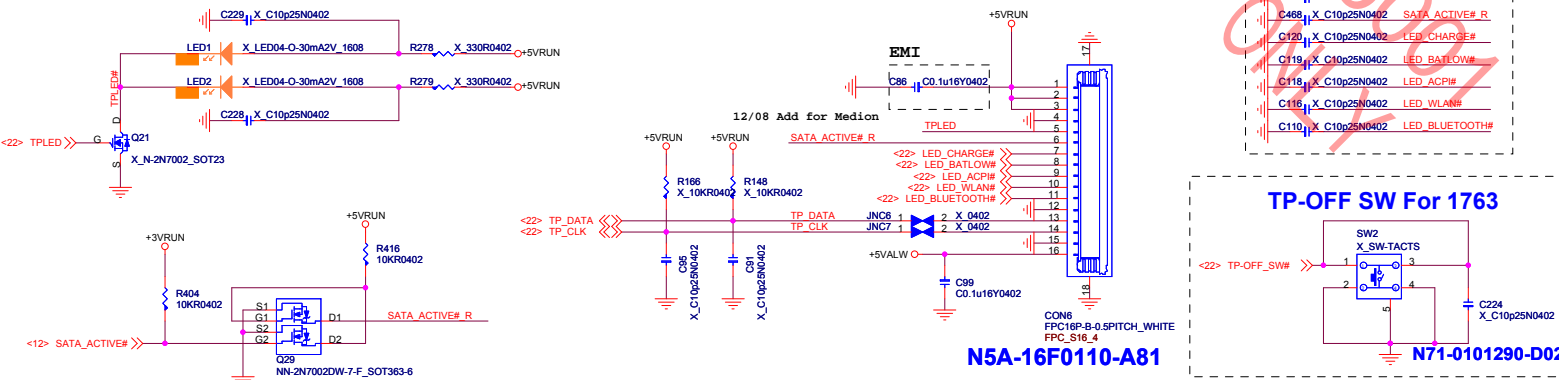
Card Reader(RTS5227)

RTS5249 Colay RTS5227

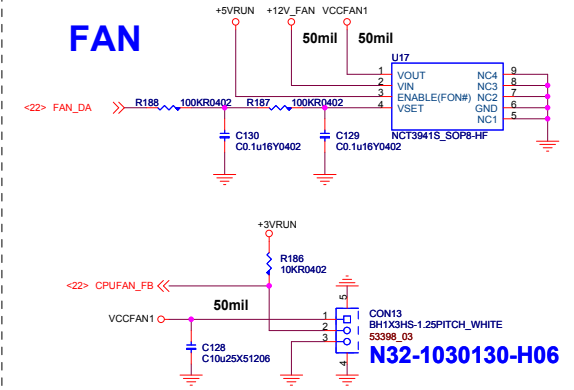
Pin 13/15/16/22/23/24/25/26 definition are different from RTS5227



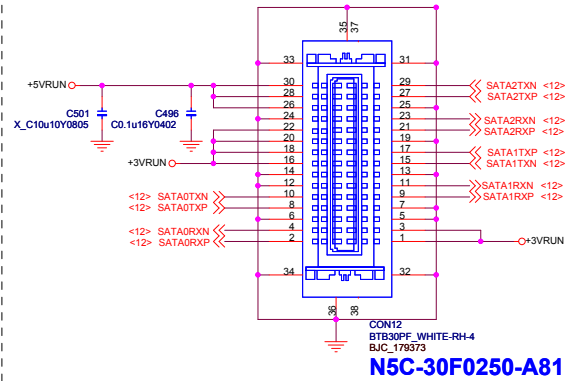
Touch Pad L/R-LED (Unmount)



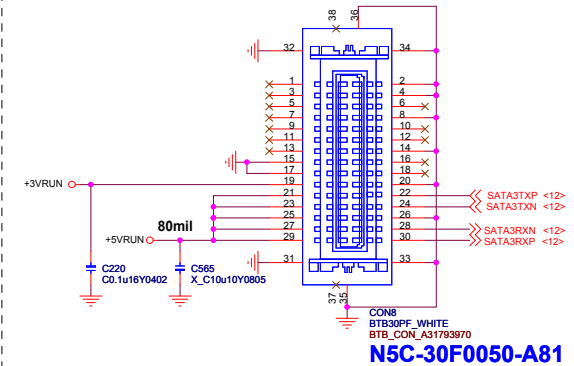
FAN



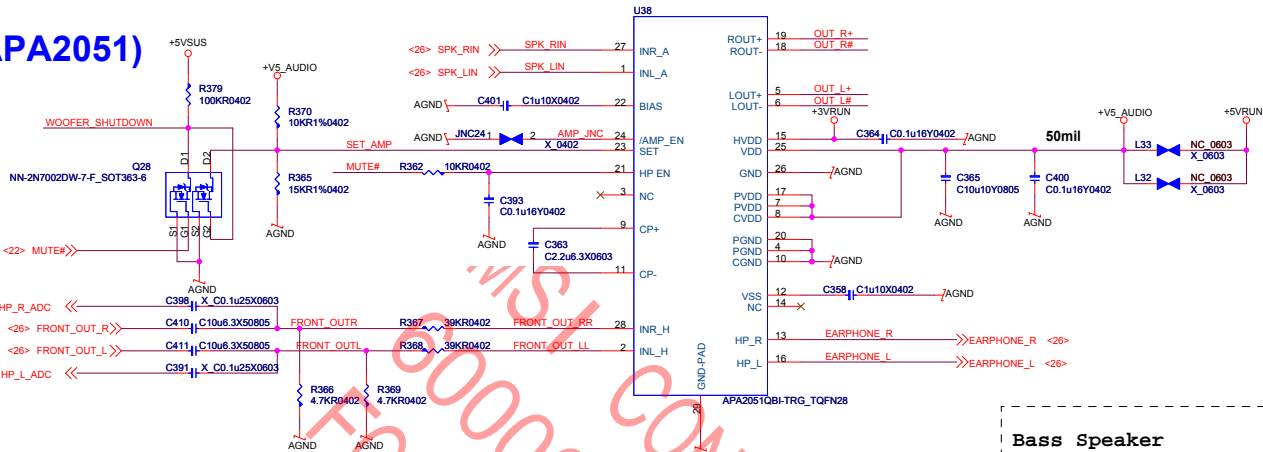
SATA HDD2 From Port 0,1,2



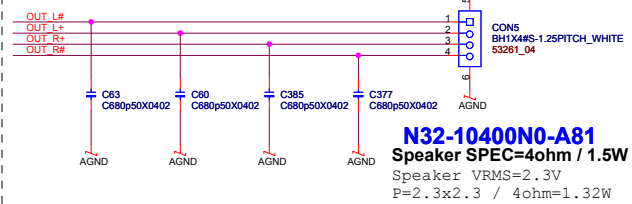
SATA HDD1 From Port 3



Audio Amp(APA2051)

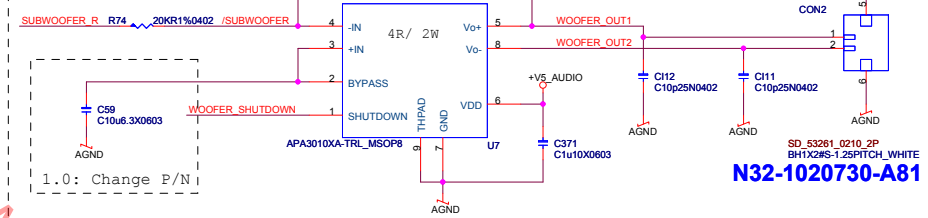


Speaker Conn

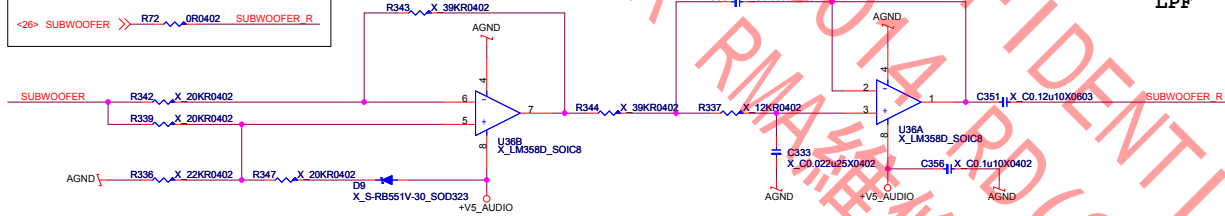


Bass Speaker

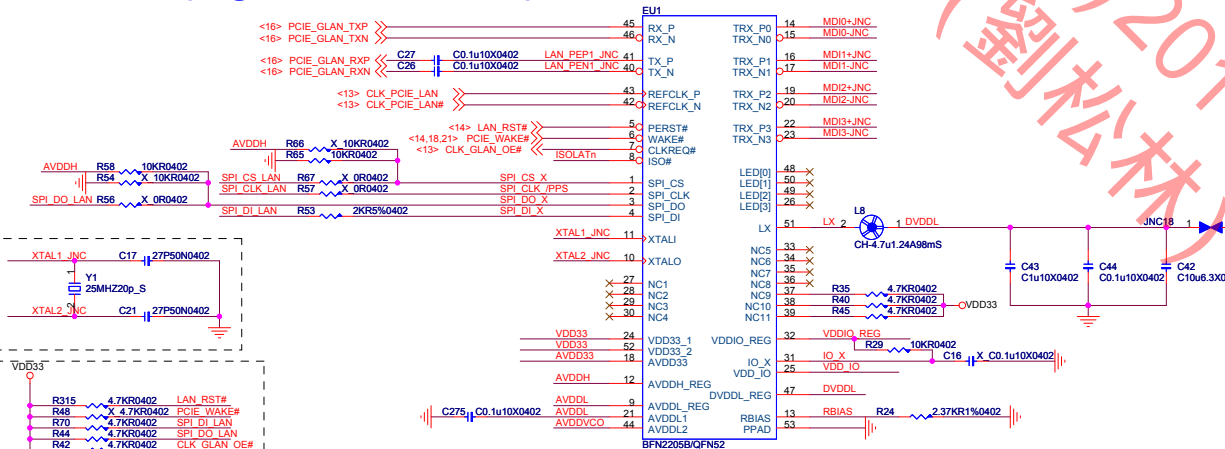
R26 = 30K RMS=3.38V
27K RMS=3.04V
24.9K RMS=2.81V



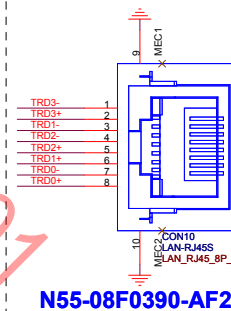
Cost Down



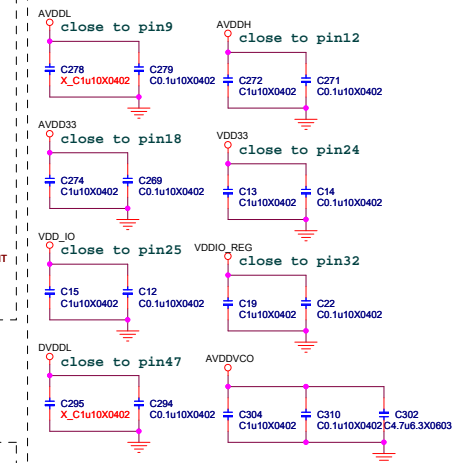
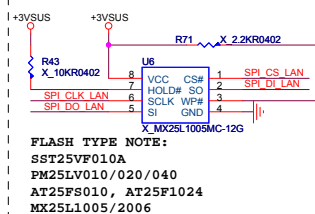
GIGA LAN(Big Foot BFN2200B)



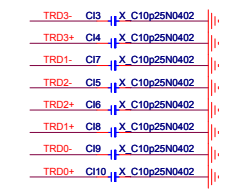
N55-08F0390-AF2



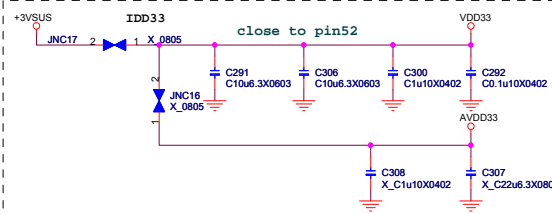
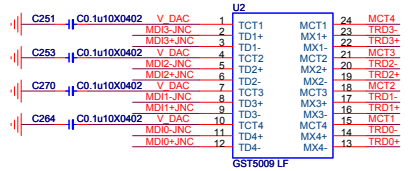
SPI ROM



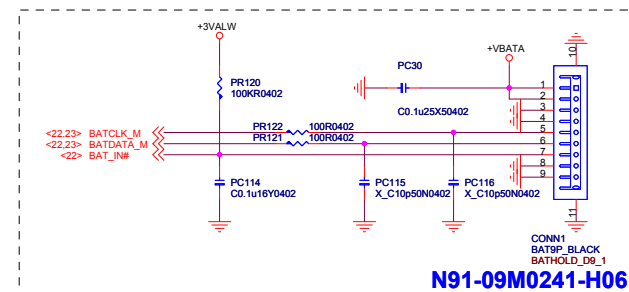
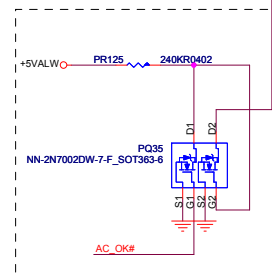
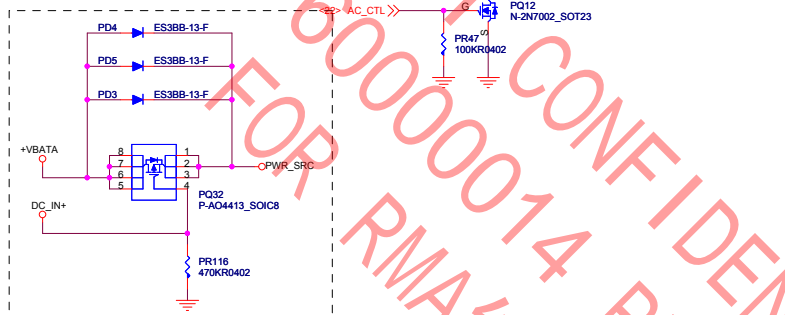
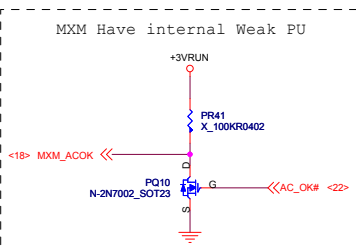
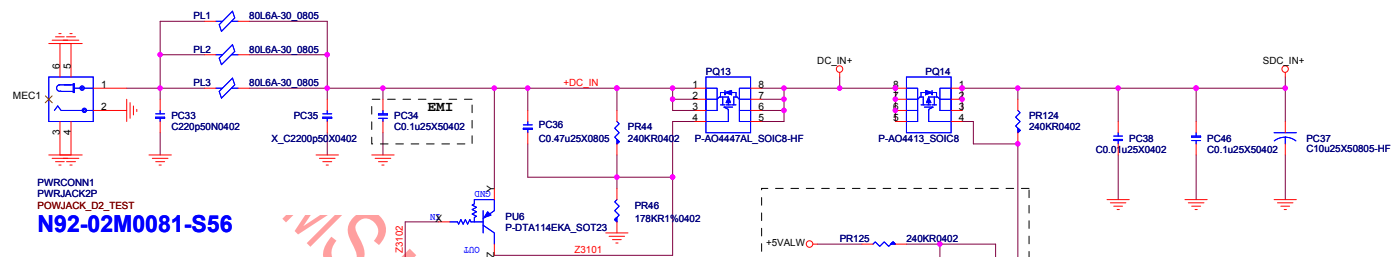
ENSWREG:ENABLE SWITCH LDO



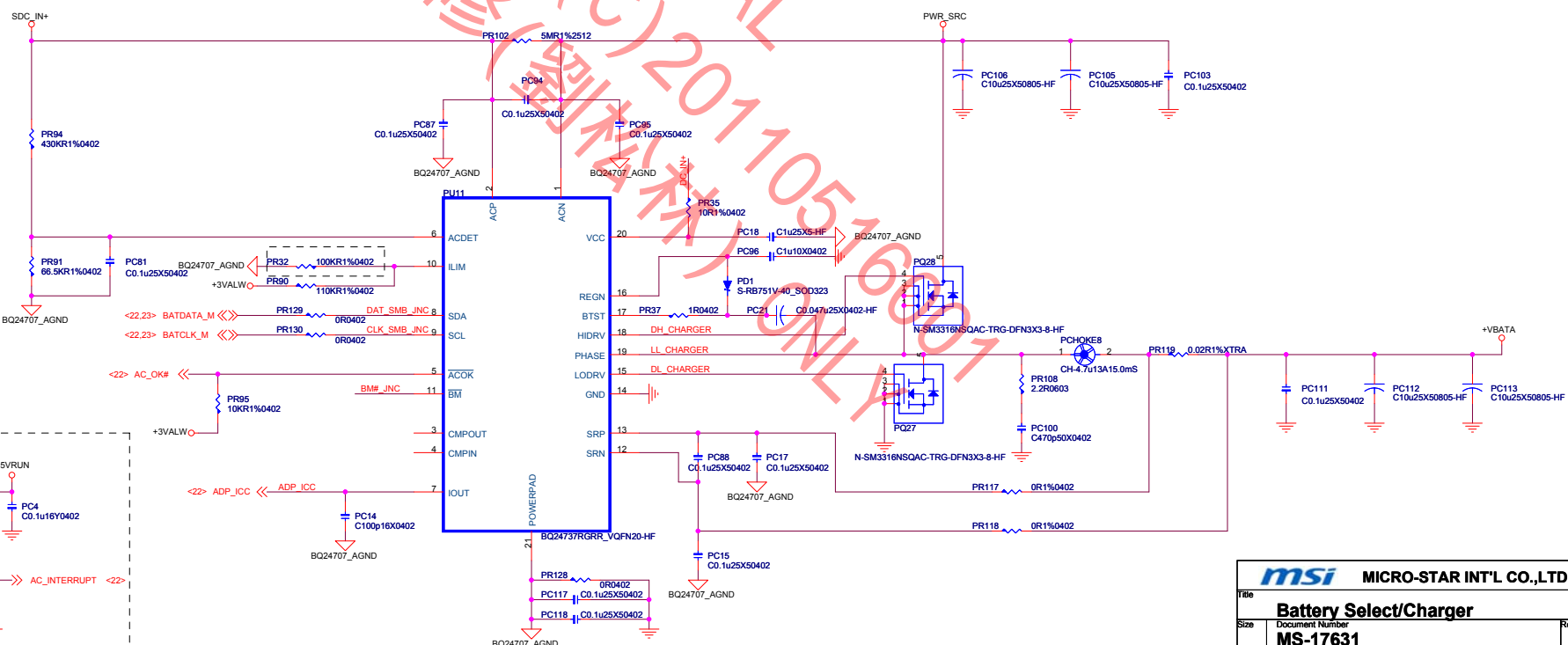
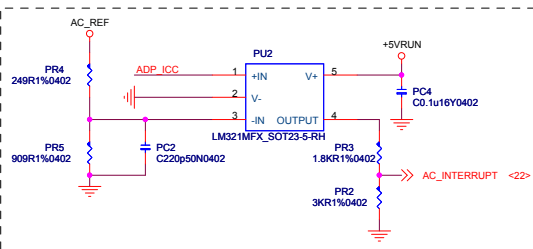
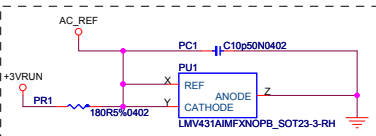
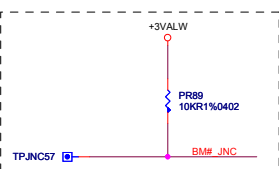
Transfer Mode



Battery Select



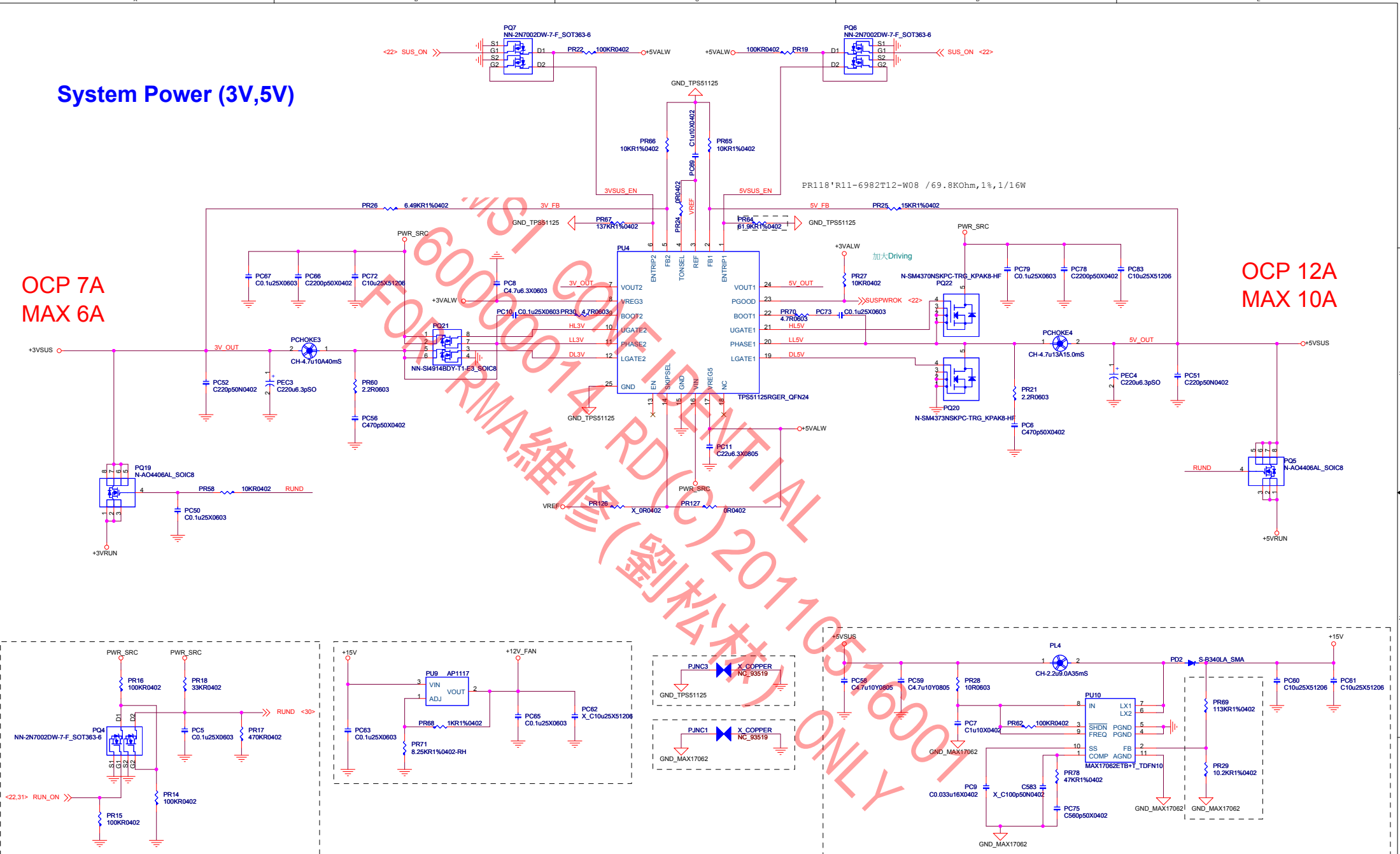
Battery Charger



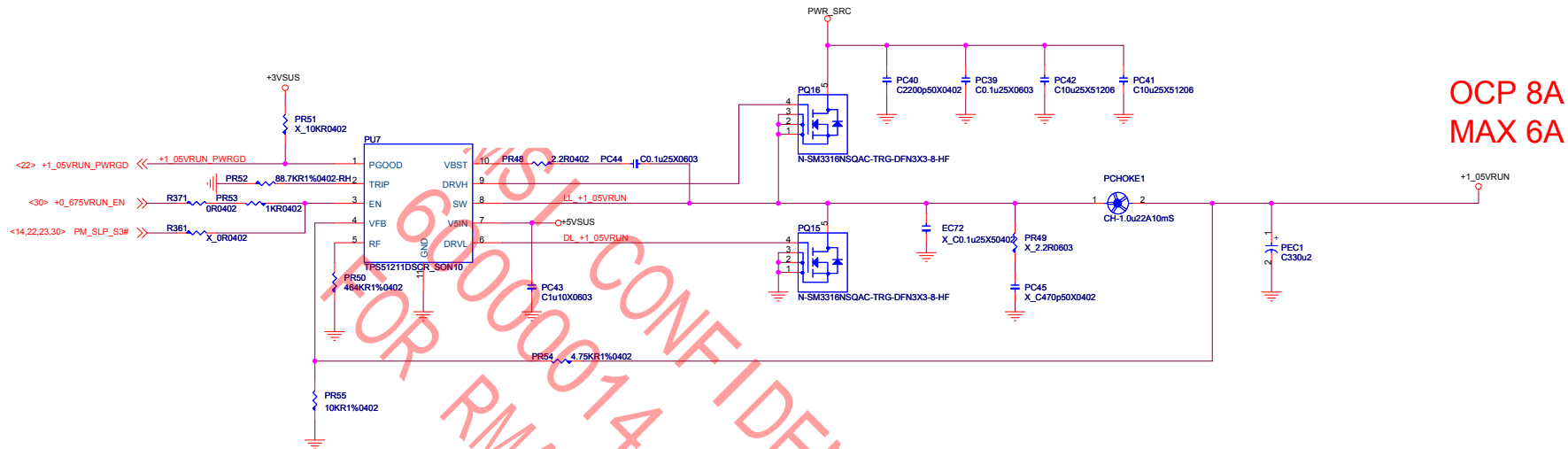
System Power (3V,5V)

OCP 7A
MAX 6A

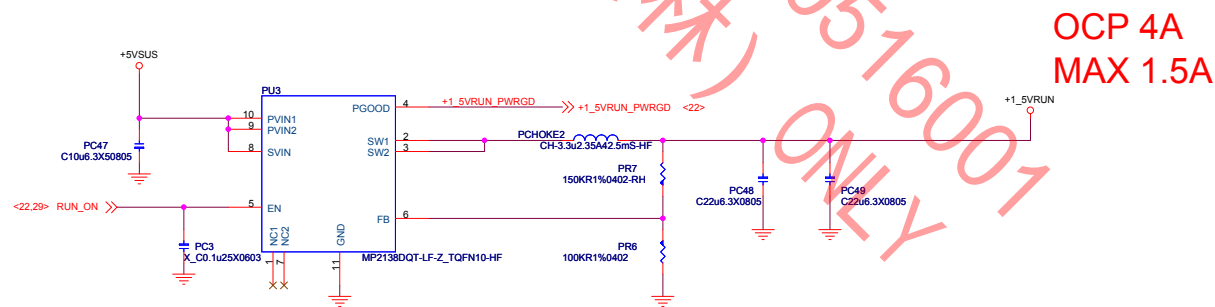
OCP 12A
MAX 10A



+1.05VRUN

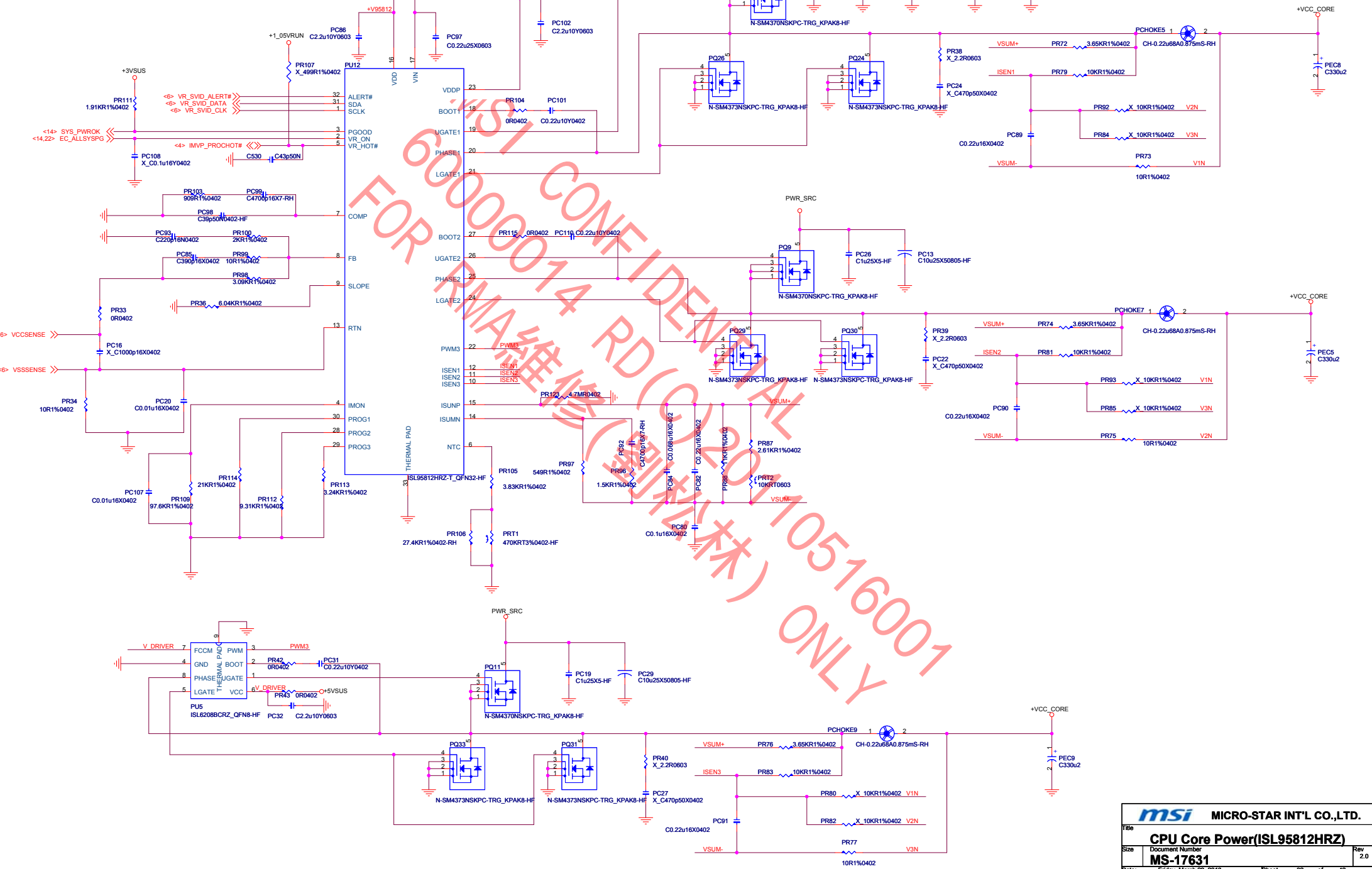


+1.5VRUN

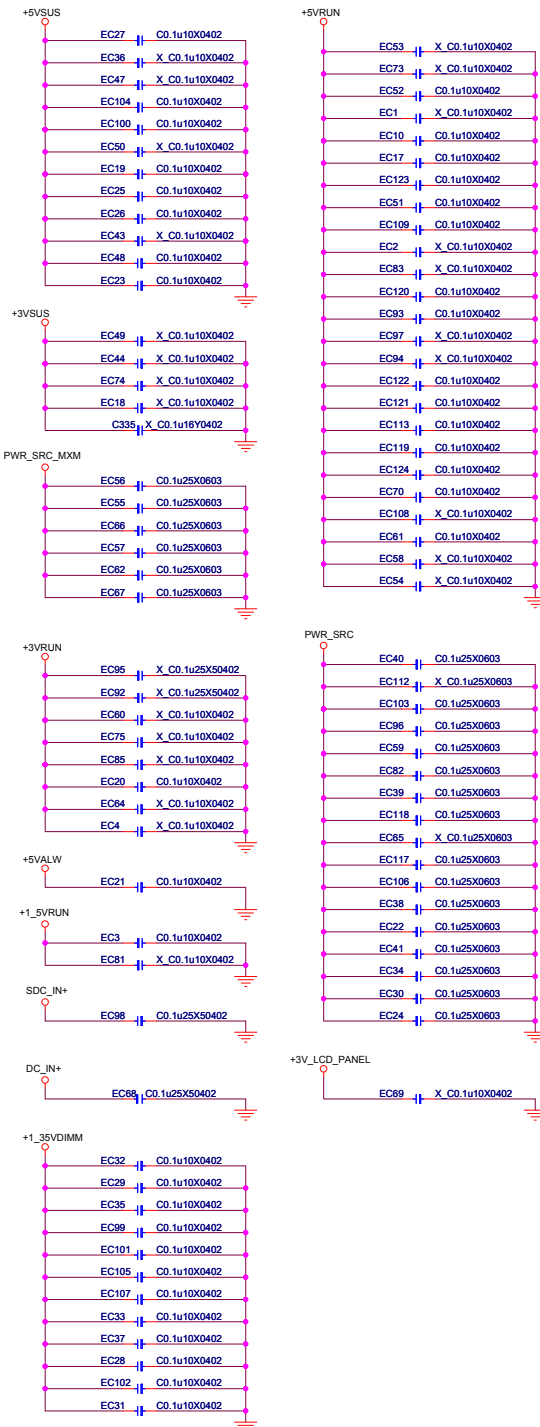


CPU Core Power(ISL95812HRZ)

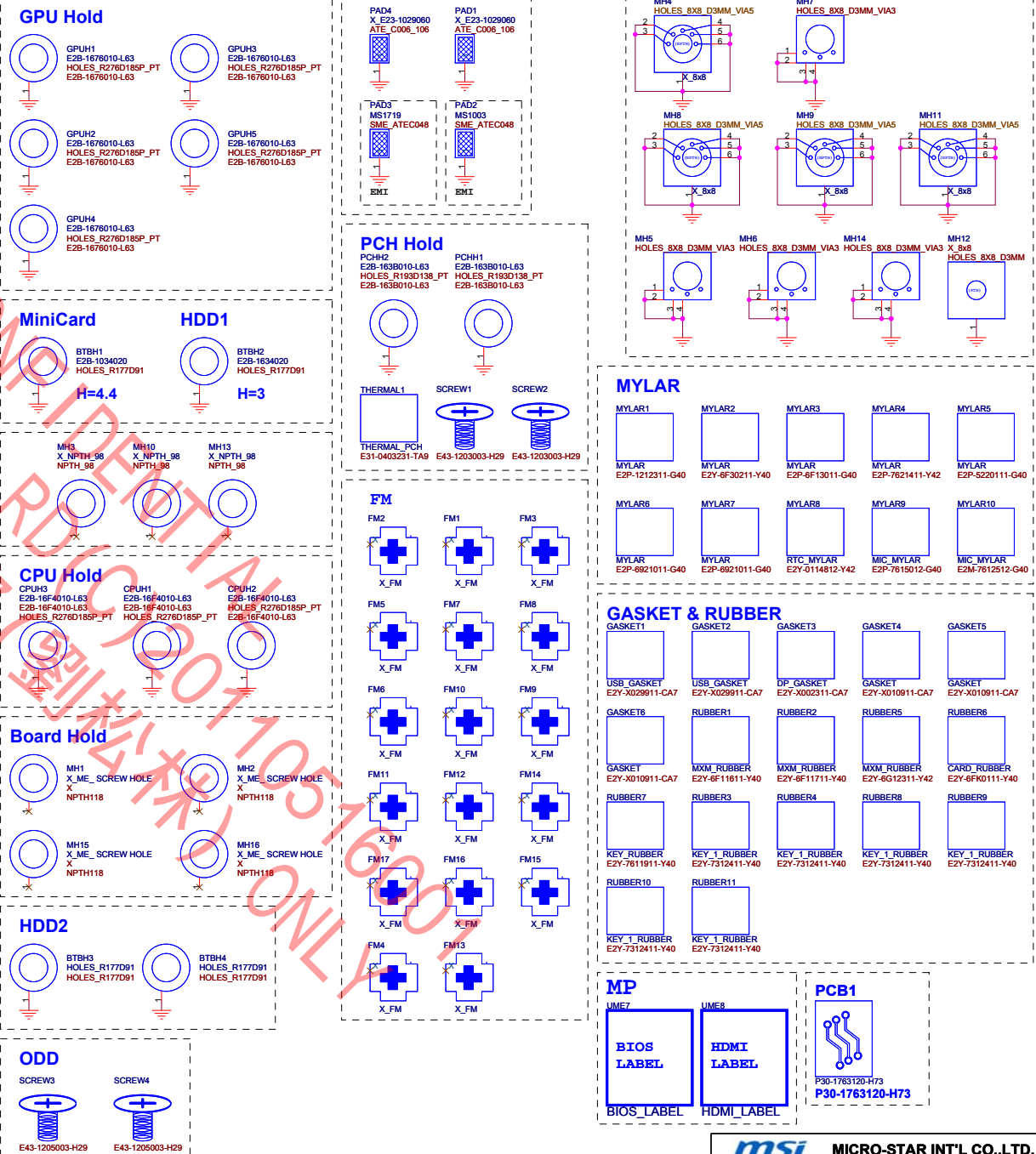
MAX 95A



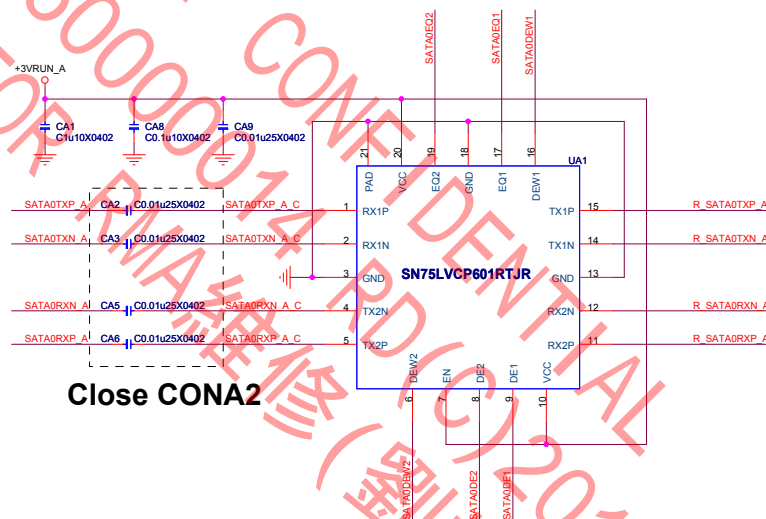
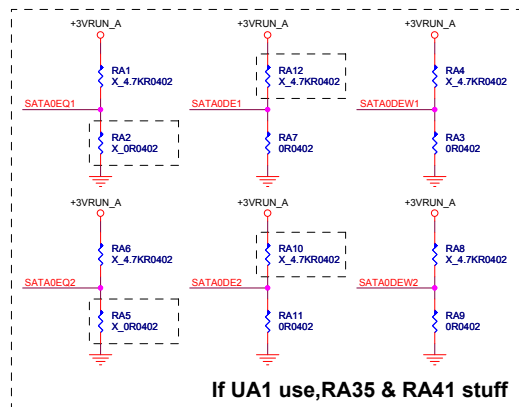
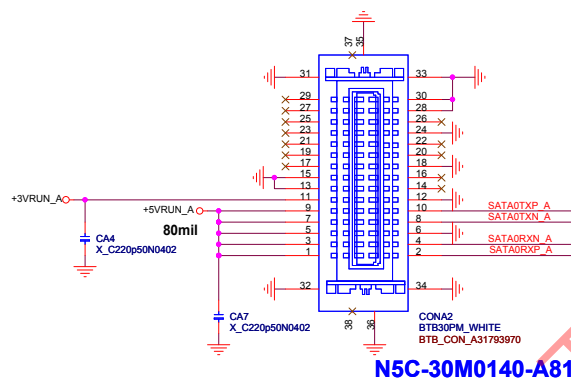
EMI



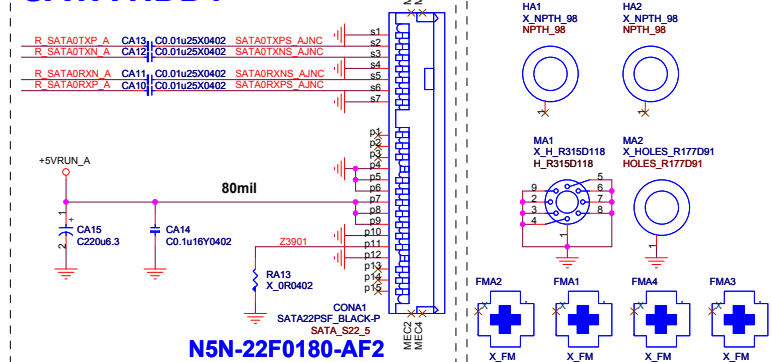
Screw



BTB Conn From Port 3



SATA HDD1



TI SN75LVCP601RTJR HW Setting

EQ1/EQ2	CH1/CH2Equalization dB (@6Gbps)	DE1/DE2	CH1/CH2De-Emphasis dB(@6Gbps)
NC (default)	0	NC (default)	-6
0	7	0	0
1	14	1	-3

DEW1/DEW2	Device Function→ DE Width for CH1/CH2
0	De-Emphasis Pulse Width Short (recommended setting when link operates at SATA 1.5/3.0/6.0 Gbps)
1 (default)	De-Emphasis Pulse Width Long (recommended setting when link operates at SATA 1.5/3.0 Gbps speed only)

MS-1763A Change List

Date	Page	Description	Date	Page	Description	Date	Page	Description

msi

MICRO-STAR INT'L CO.,LTD.

Title

HDD1

Size

Document Number

MS-1763A

Date:

Friday, March 28, 2013

Sheet

34

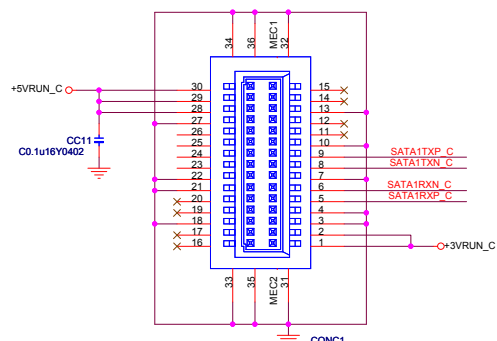
of

49

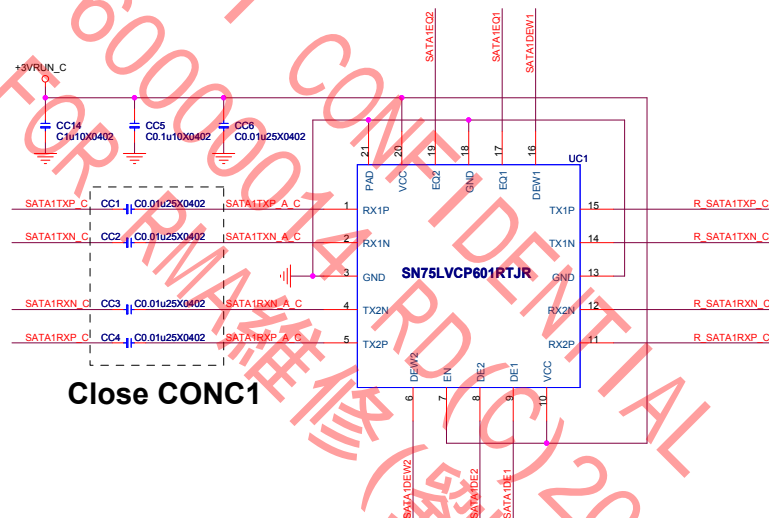
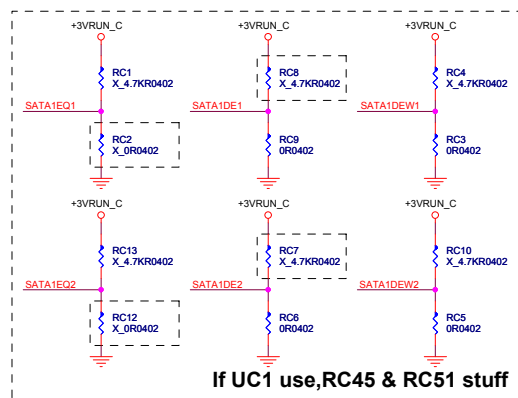
Rev

2.0

BTB Conn From Port 1

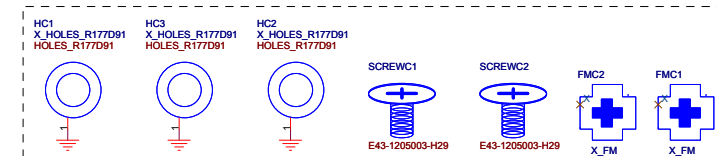
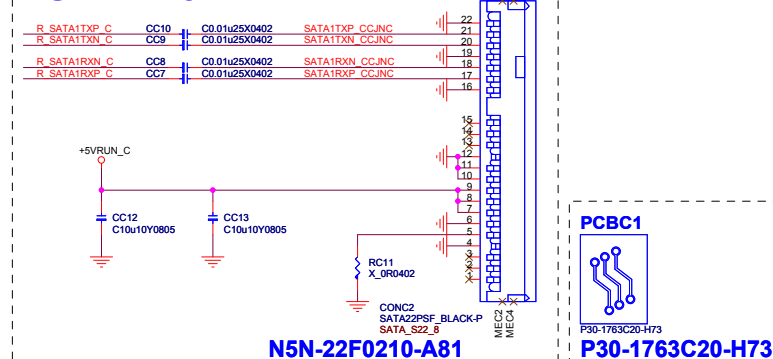


N5C-30M0170-A81



Close CONC1

SATA Conn



TI SN75LVCP601RTJR HW Setting

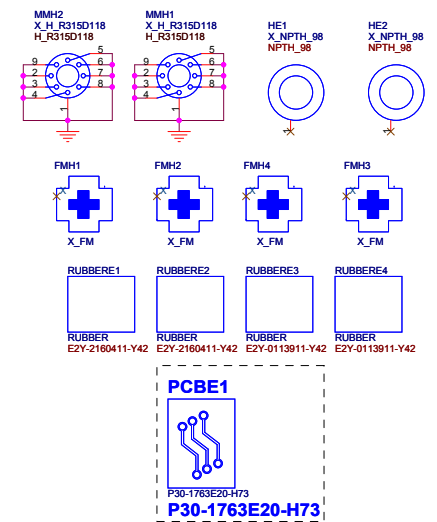
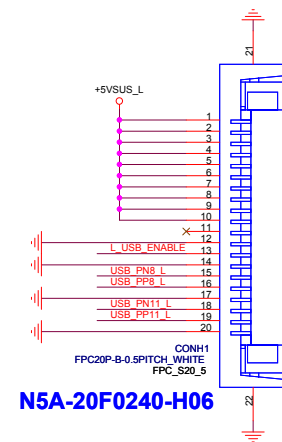
EQ1/EQ2	CH1/CH2Equalization dB (@6Gbps)	DE1/DE2	CH1/CH2De-Emphasis dB(@6Gbps)
NC (default)	0	NC (default)	-6
0	7	0	0
1	14	1	-3

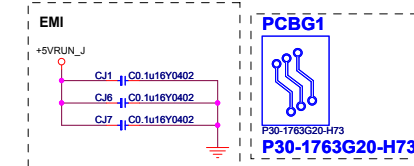
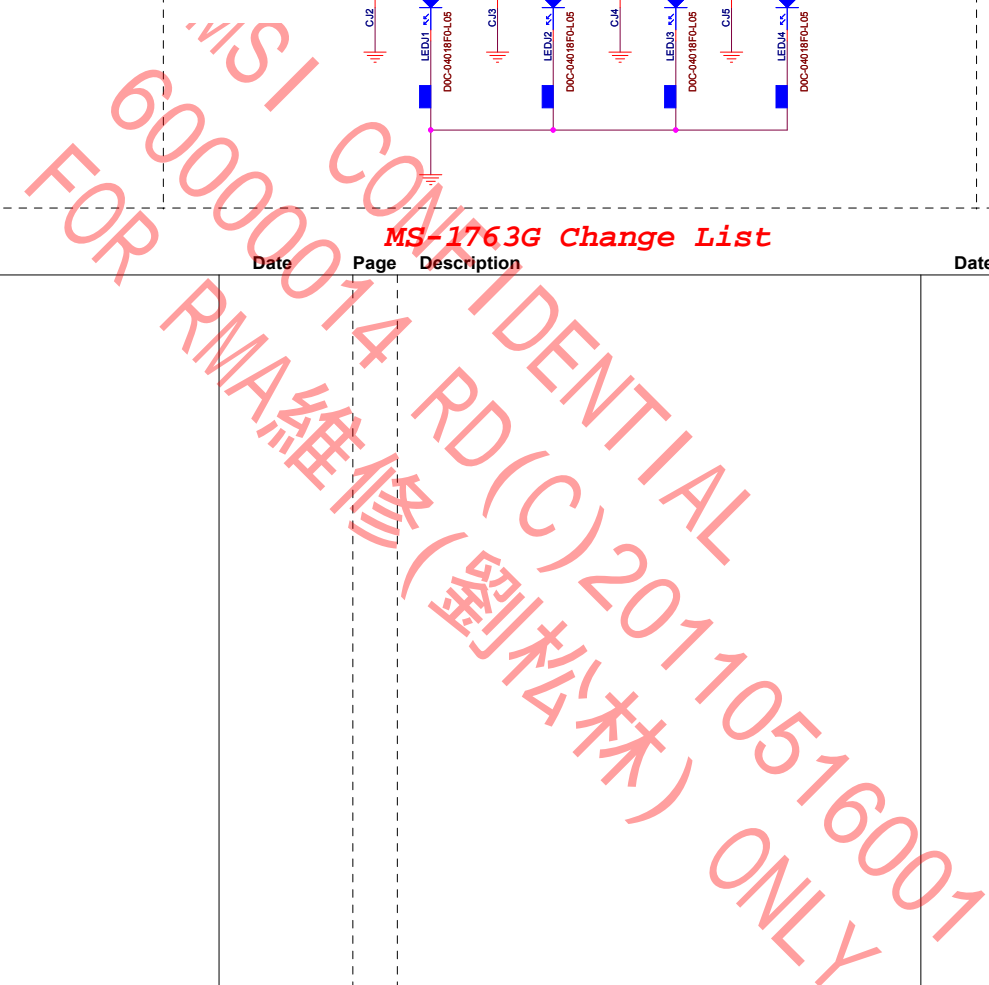
DEW1/DEW2	Device Function→ DE Width for CH1/CH2
0	De-Emphasis Pulse Width Short (recommended setting when link operates at SATA 1.5/3.0/6.0 Gbps)
1 (default)	De-Emphasis Pulse Width Long (recommended setting when link operates at SATA 1.5/3.0 Gbps speed only)

MS-1763C Change List


[illegible]

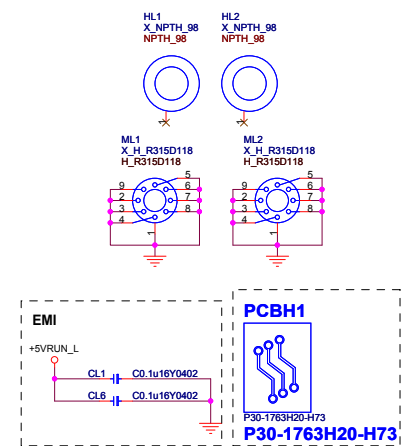
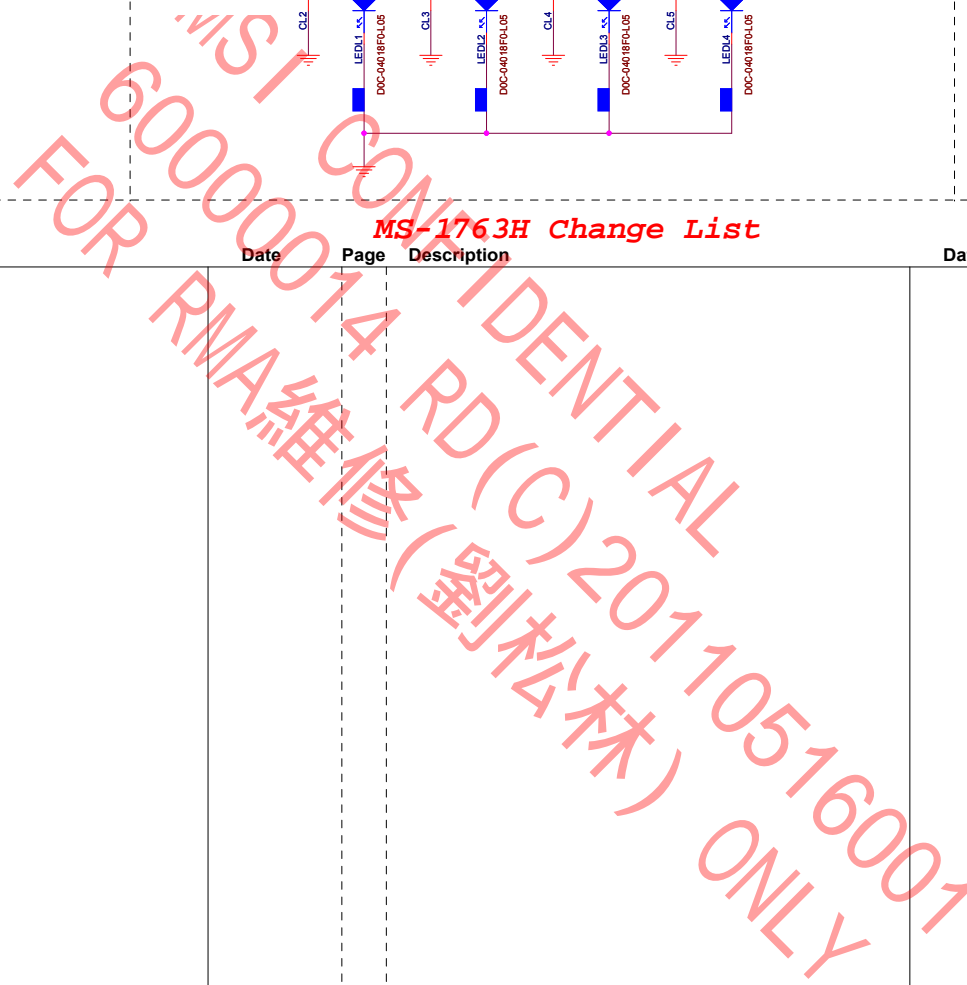
The schematic diagram illustrates the internal circuitry of the USB to RS-485 module. It features a USB interface on the left, connected to a USB to UART module (GM8255) in the center, and an RS-485 interface on the right. The USB interface includes a USB connector (USBH1) and a USB to UART module (GM8255) with pins for USB5V, PT1_L, and PT1_R. The RS-485 interface includes an RS-485 connector (ECH1, ECH2, ECH3) and an RS-485 transceiver (CMC_L12-9008084). The module is powered by a 5V USB supply (5VSUS_L) and includes various capacitors for decoupling and timing. The module is labeled N53-04M0411-H06.

[illegible][illegible]




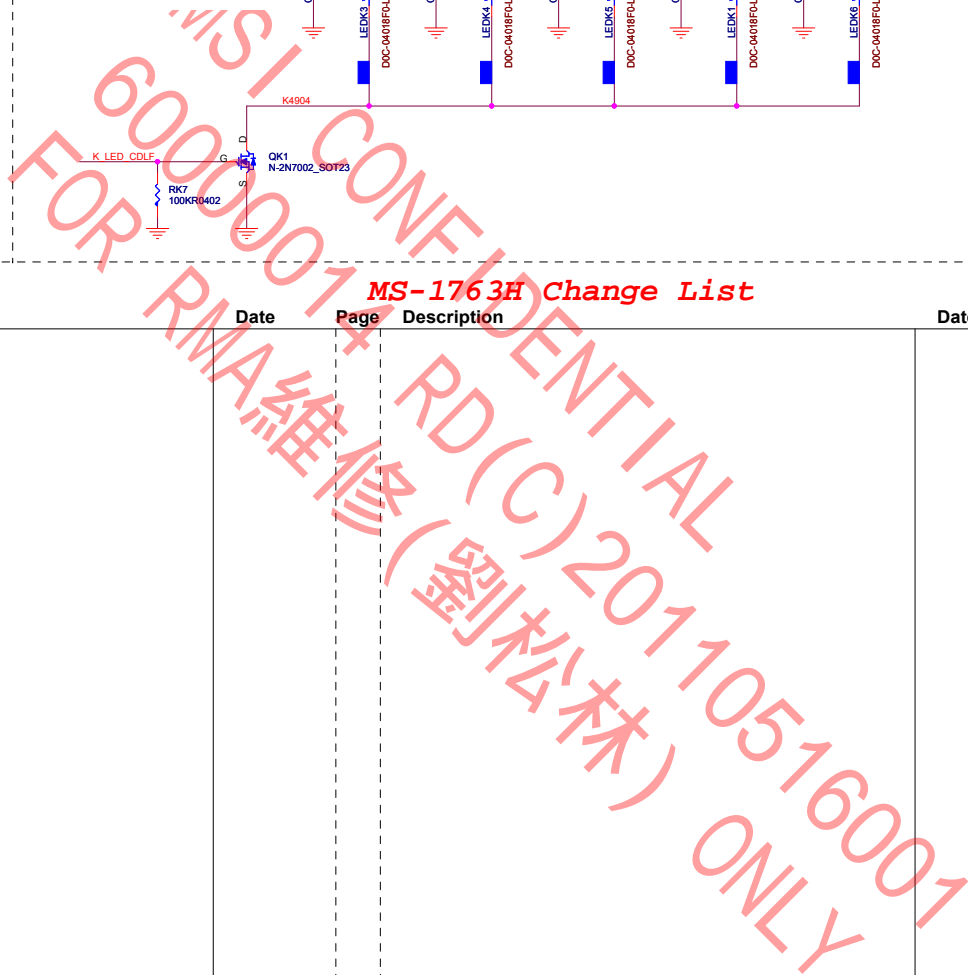
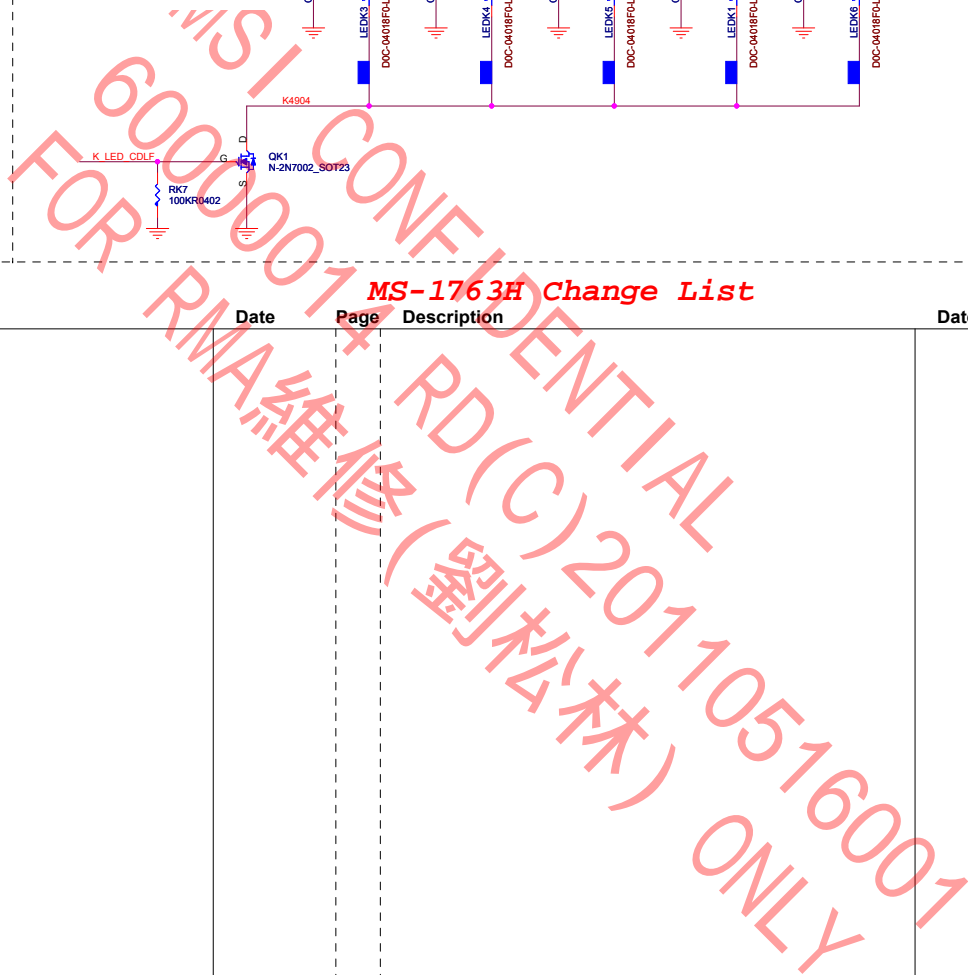
MS-1763G Change List				Date
Date	Page	Description		

 MICRO-STAR INT'L CO.,LTD.	
Title	
SPK L LED	
Size	Document Number MS-1763G
Date:	Friday, March 29, 2013 Sheet 40 of 49 Rev 2.0



MS-1763H Change List			Date	Page	Description

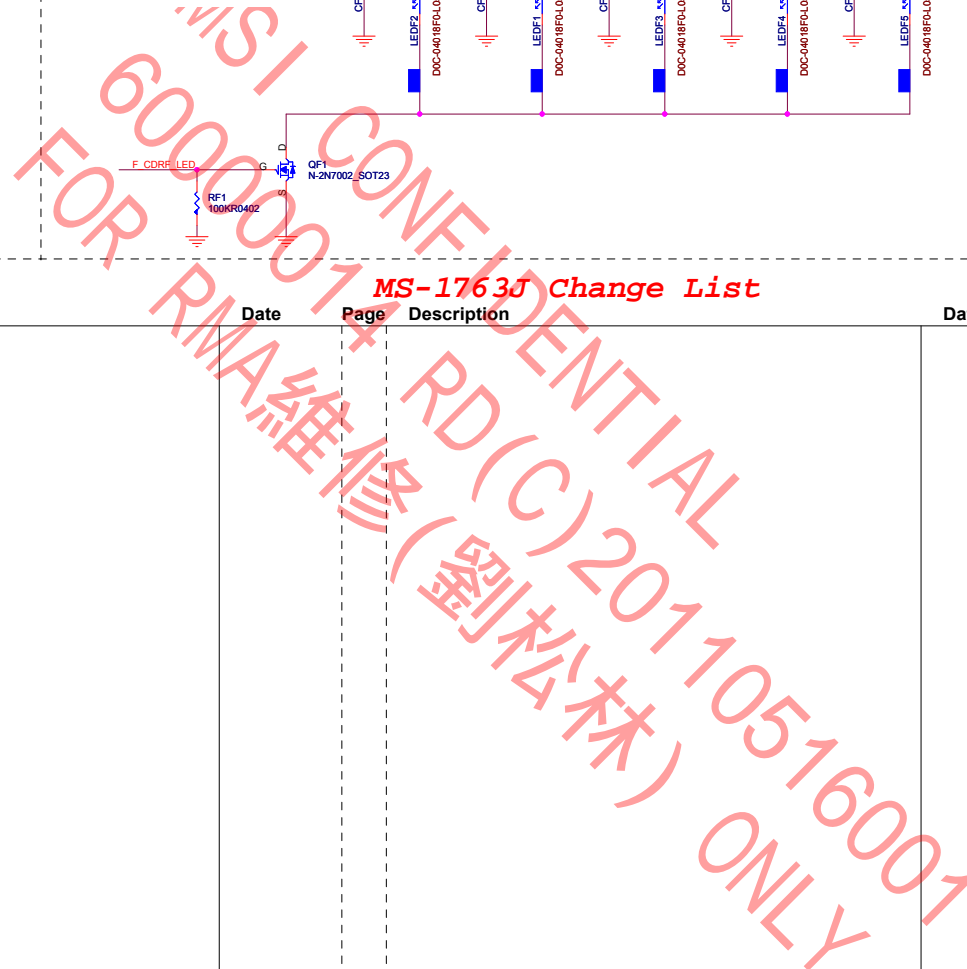
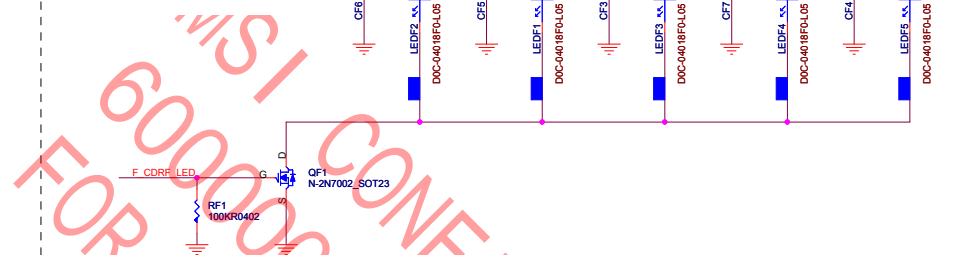
		MICRO-STAR INT'L CO.,LTD.	
Title			
SPK R LED			
Size	Document Number	Rev	
	MS-1763H	2.0	
Date:	Friday, March 29, 2013	Sheet	41 of 49



MS-1763H Change List

Date	Page	Description	Date

[illegible]



Date	Page	Description	Date	Page	Description	Date	Page	Description

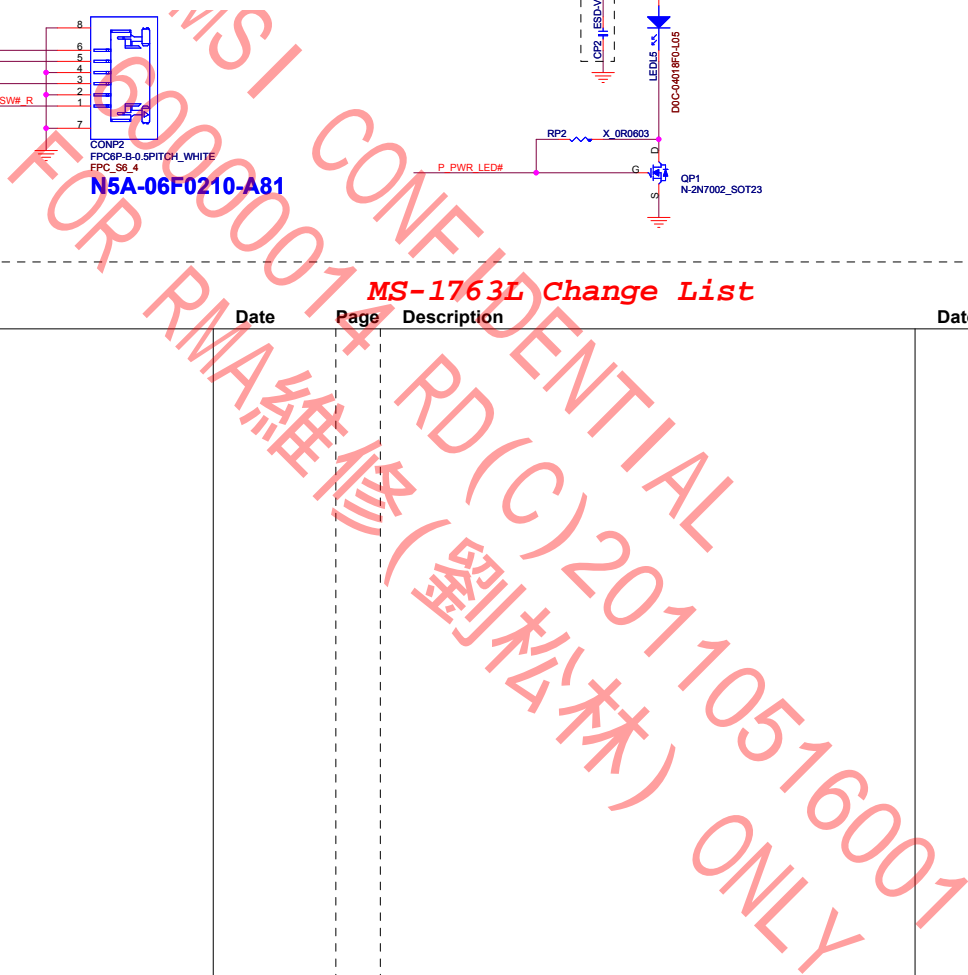
MSI
CD LED RF

MS-1763J

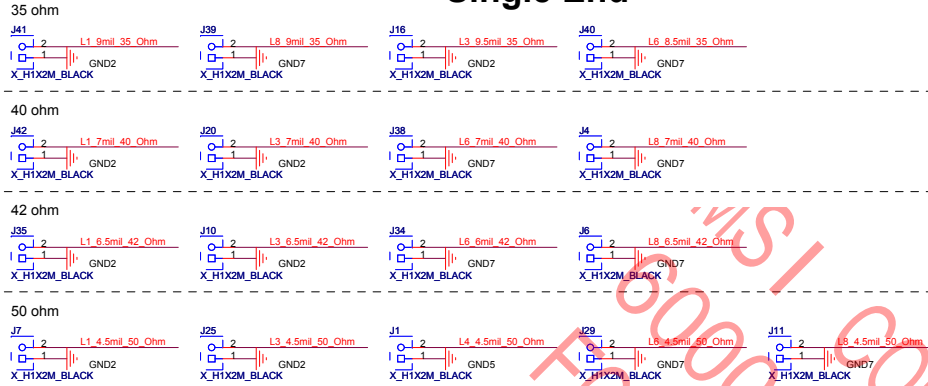
Rev 2.0

Friday, March 29, 2013

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[illegible]

Impedance Single End

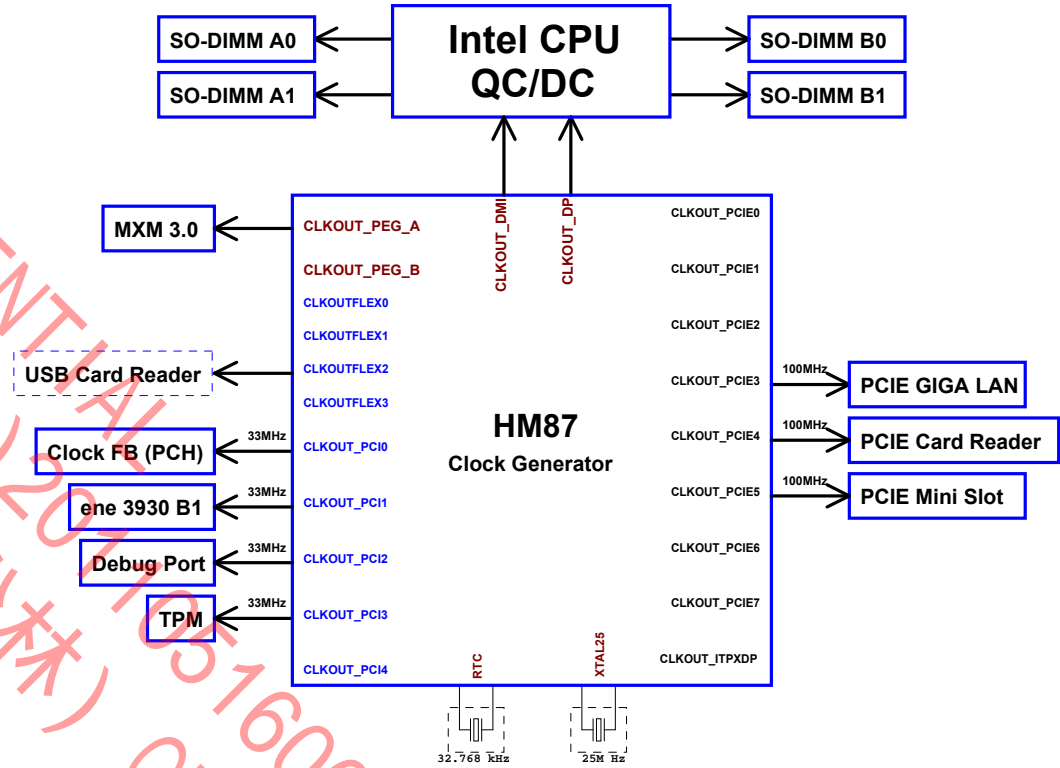


Differential



Clock Distribution

Internal Clock Mode



Power on Sequence

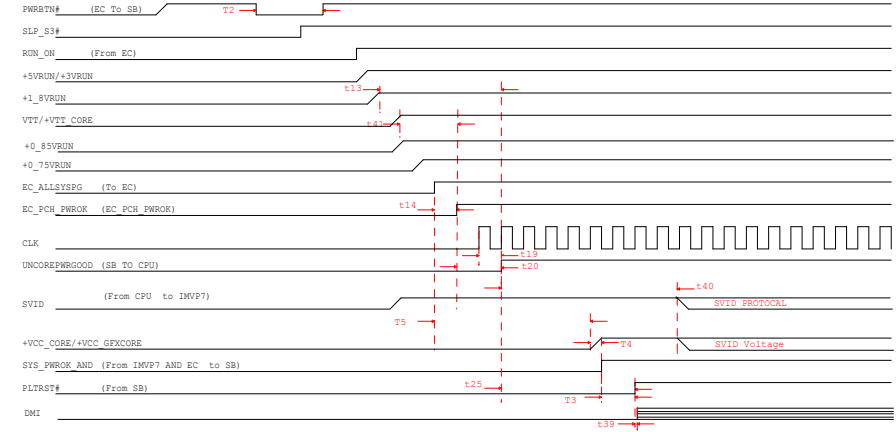
S5-S0

EC programming timing



S3-S0

EC programming timing

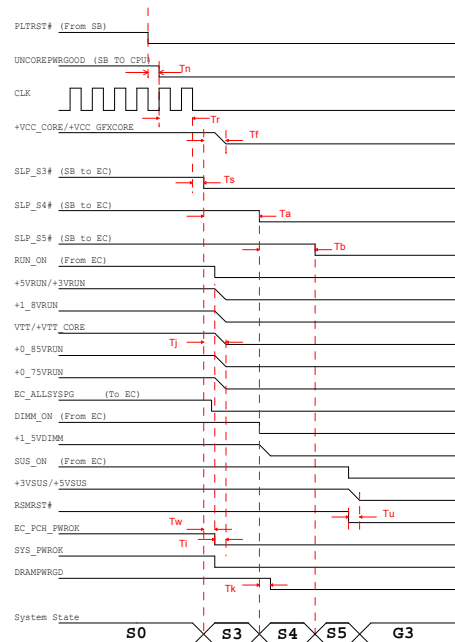


	Min	Max	Unit	Description
T1	150		mS	
T2	16		mS	
T3	1		mS	Timing set by PCH
t04	10		mS	
t07	100		mS	
t08		90	mS	
t09	30		uS	
t10	30		uS	
t13	5	650	mS	
t14	99		mS	EC Delay
t17	2	650	mS	
t18	1		mS	Timing set by PCH
t19	41		mS	Timing set by PCH
t20	2		mS	Timing set by PCH
t25	1	100	mS	
T5		800	uS	Follow MVP Spec
T4	2.5		mV/uS	Follow MVP Spec
t39		200	uS	
t40		500	uS	
t41	10		mS	

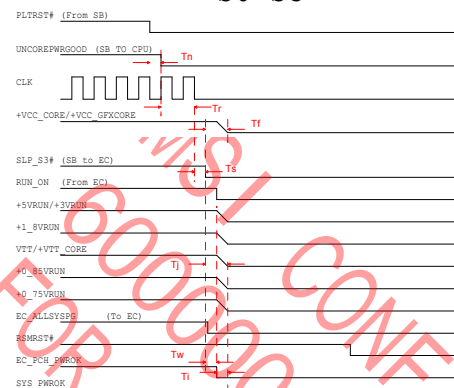
Power down Sequence

S0-S5

EC programming timing

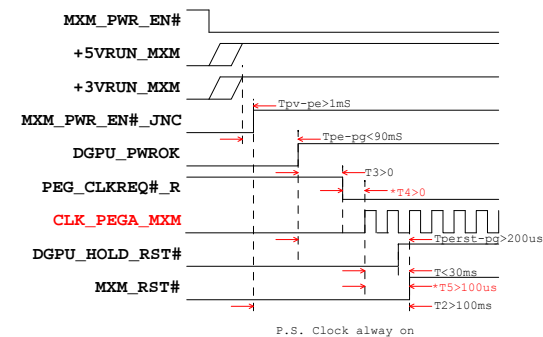


S0-S3

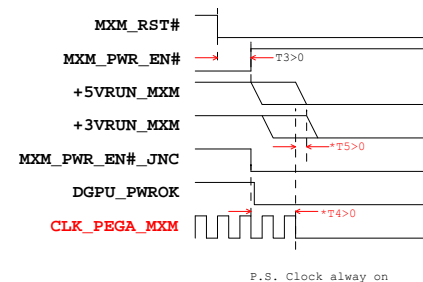


	Min	Max	Unit	Description
Ta	30		uS	
Tb	30		uS	
Tf		500	mS	
Ti	40		nS	
Tj	5		uS	
Tk	100		nS	
Tn	30		uS	
Tp	500		uS	Sx-RSMRST#
Tr	10		uS	
Trs	1		uS	
Tu	40		nS	
Tw	0		mS	

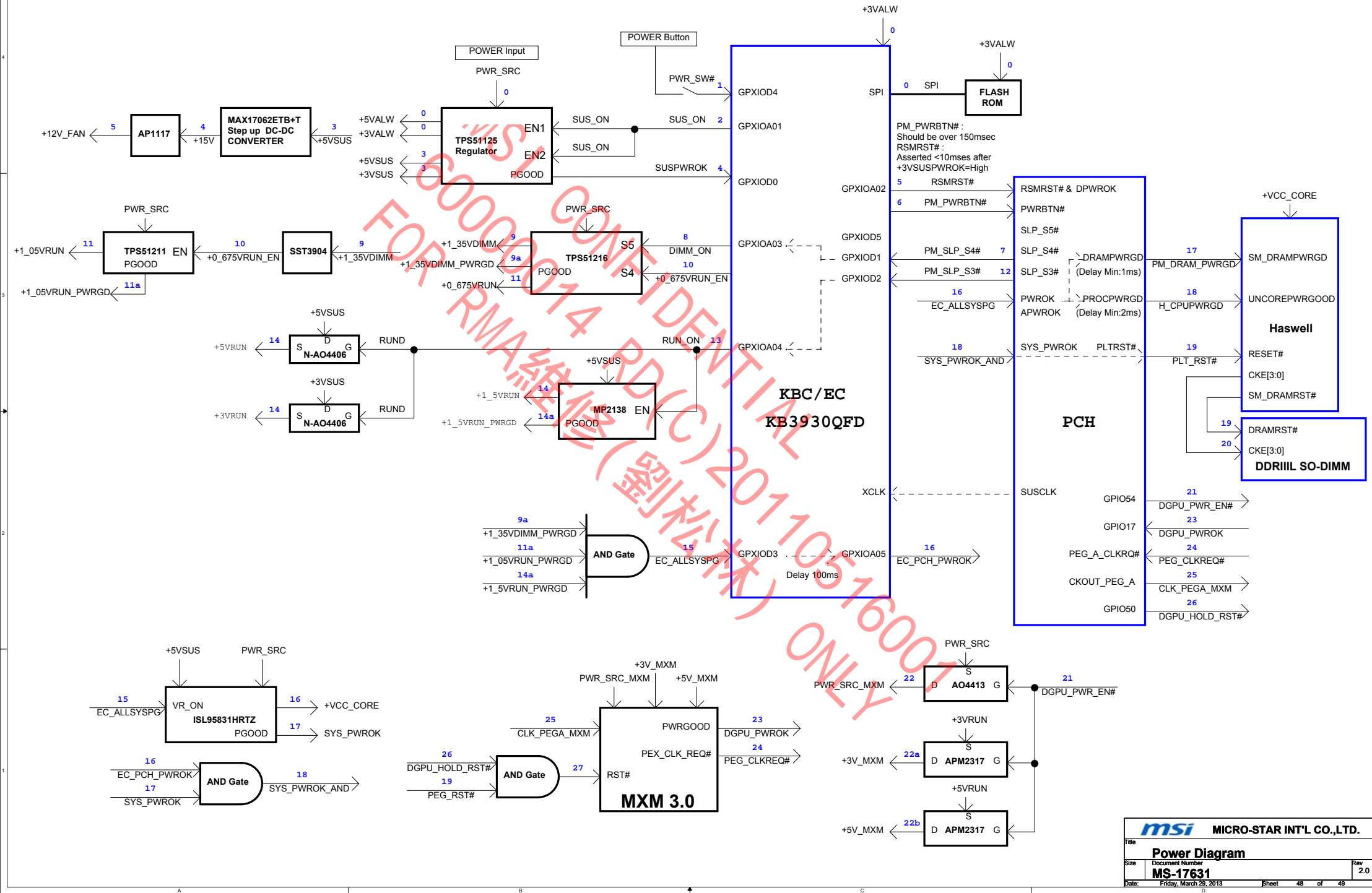
Power-Up Sequence For Optimus On MXM



Power-Down Sequence For Optimus On MXM



Power Diagram



DC_IN
Adaptor 180W

BQ24737
Charger

ISL95812HRZ
+VCC_CORE

TPS51216RUKR
+1_35VDIMM

TPS51211DSCR
+1.05V

TPS51125RGER
+3VALW/+5VALW

N MOS
SM4370N

N MOS
SM4373N

N MOS
SM4370N

N MOS
SM4373N

N MOS
SM3316N

N MOS
SM3316N

N MOS
SI4914BDY

N MOS
SM4370N

N MOS
SM4373N

+VCC_CORE / 85A

+1.35VDIMM / 16.2A

+1.05VRUN / 6.68A

+3VSUS / 9.586A

+5VSUS / 21.2A

N MOS
AO4406AL

N MOS
AO4406AL

MAX17062ETB+T
+15V

MP2138DQT
+1.5VRUN

+3VRUN / 7.733A

+5VRUN / 6.5A

+15V / 2.16A

+1.5VRUN / 624mA

AP1117
+12V

+12V / 2.7A

+0.675VRUN / 2A

+3VALW / 20mA

KB3930QFB1	
VCC	3.3VALW 20mA

MXM 3.1	
PWR_SRC	19V 10A
3.3V	3VRUN 1A
5V	5VRUN 2.5A

ANX1122	
3.3V	3VRUN 0.081mA
1.05V	1.05VRUN 0.11mA

TPM	
VS	3VSUS 25mA
VDD	3VRUN 5mA

Camera	
VCC	3VRUN 350mA

MCU	
VCC	3VRUN 25mA

P2501	
VCC	3VRUN 25mA

Haswell (rPGA 947)	
VCC_CORE	1.2V 85A
VDDQ	1.35V 4.2A
Lynx Point HM87	
VCC3_3	3.3V 223mA
VCCIO	1.05V 6.67A
VCCVRM	1.5V 179mA
VCCDSW	3.3V 286mA
VCCADAC	1.5V 70mA
DDR 3L	
VDDQ	1.35VDIMM 12A
VREF	0.675VRUN 2A
LVDS	
VDD	3.3VRUN 2A
VLED	19V 1.5A
Realtek RTS5209	
3V3_IN	3VRUN 300mA
CPU FAN	
VCC	12V 2.7A
ALC892-CG	
VDD33	3VSUS 1mA
AVDD	5VSUS 60mA
DVDD	3VSUS 41mA
Amplifier	
VDD	5VSUS 485mA
HVDD	3VRUN 5mA
Mini PCI-E	
+3.3V	3VRUN 1.1A
+1.5V	1.5VRUN 375mA
USB Ports	
USB 2.0*2	5VSUS 1.5A
USB 3.0*3	5VSUS 6A
Bigfoot E2200	
VDD33	3VSUS 1.5A
SATA Ports	
HDD	5VRUN 2A
ODD	5VRUN 2A
mSATA	3VRUN 2.7A

Power Name	Current
VCC_CORE	85A
1.35VDIMM	16.2A
0.675VRUN	2A
1.05VRUN	6.68A
3VSUS	6.886A
3VRUN	5.033A

Power Name	Current
5VSUS	21.22A
5VRUN	6.5A
15V	2.16A
12V	2.7A
1.5VRUN	624mA
3VALW	20mA